

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHM, MLB, MBP15  
05/08/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		50282	PRODUCTION RELEASED	05/08/07	

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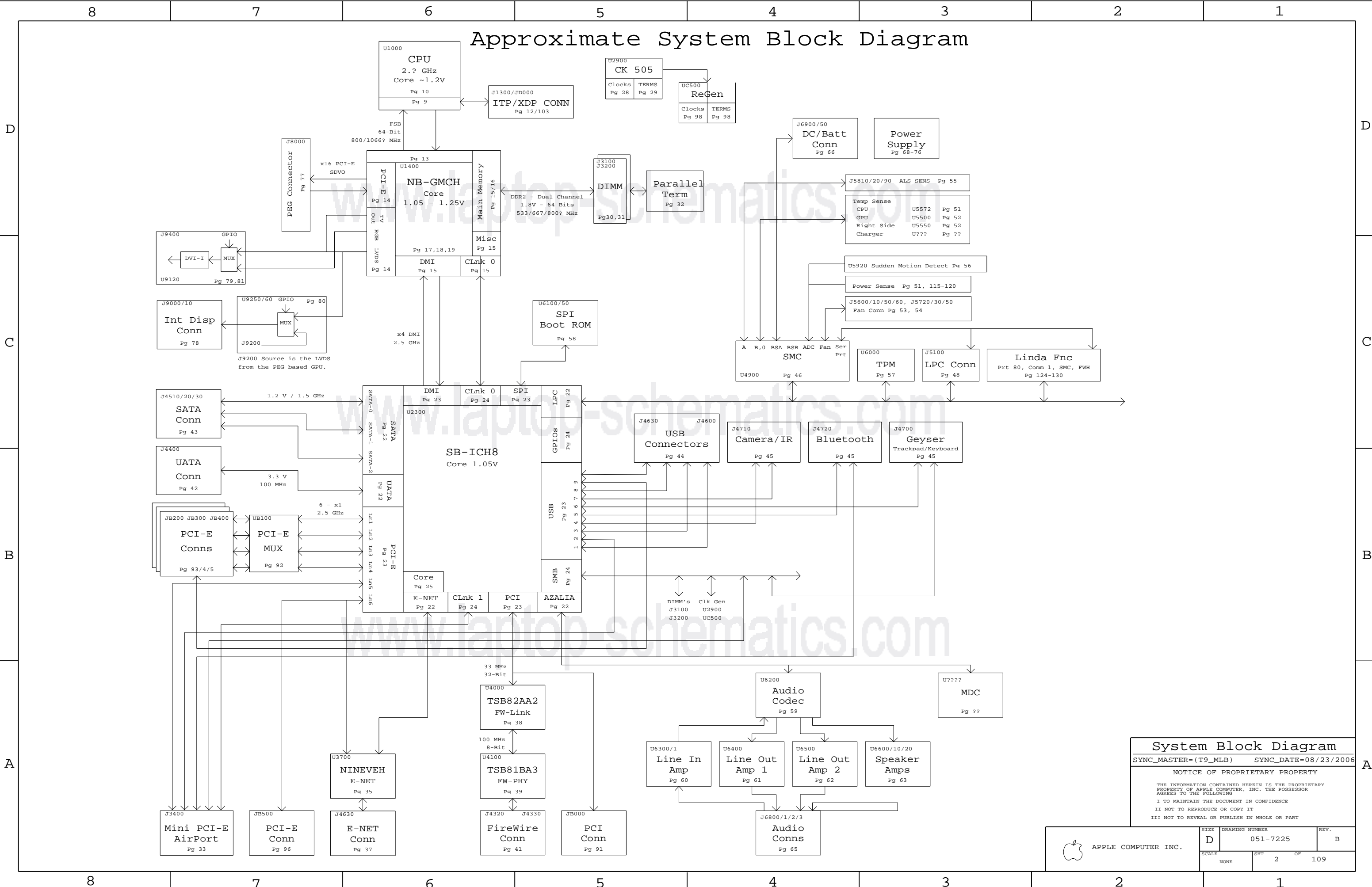
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7225	1	SCHEM,MLB,MBP15	SCH	CRITICAL	
820-2101	1	PCBF,MLB,MBP15	PCB	CRITICAL	

DRAWING  
TITLE=MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=Tue May 8 11:40:41 2007

DIMENSIONS ARE IN MILLIMETERS  XX ± _____  X.XX ± _____  X.XXX ± _____  ANGLES ± _____  DO NOT SCALE DRAWING	METRIC				<div>Apple Computer Inc.</div>	
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	ENG APPD		MFG APPD			
QA APPD		DESIGNER		TITLE		
RELEASE		SCALE NONE		SCHEM, MLB, MBP15		
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D				
<div><div></div><div>THIRD ANGLE PROJECTION</div></div>						
DRAWING NUMBER 051-7225					REV. B	
SHT 1 OF 109						

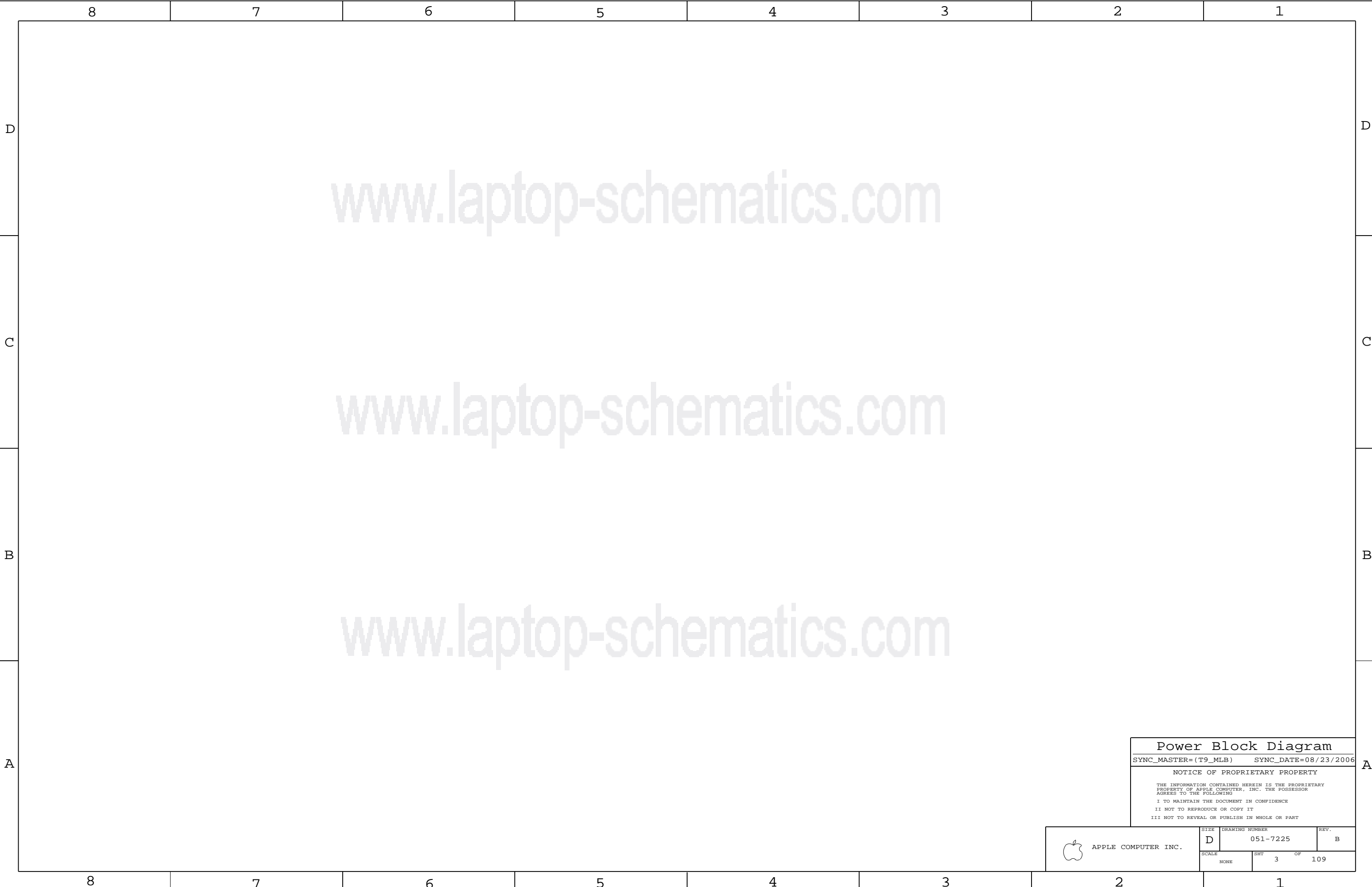


Approximate System Block Diagram


**System Block Diagram**  
SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

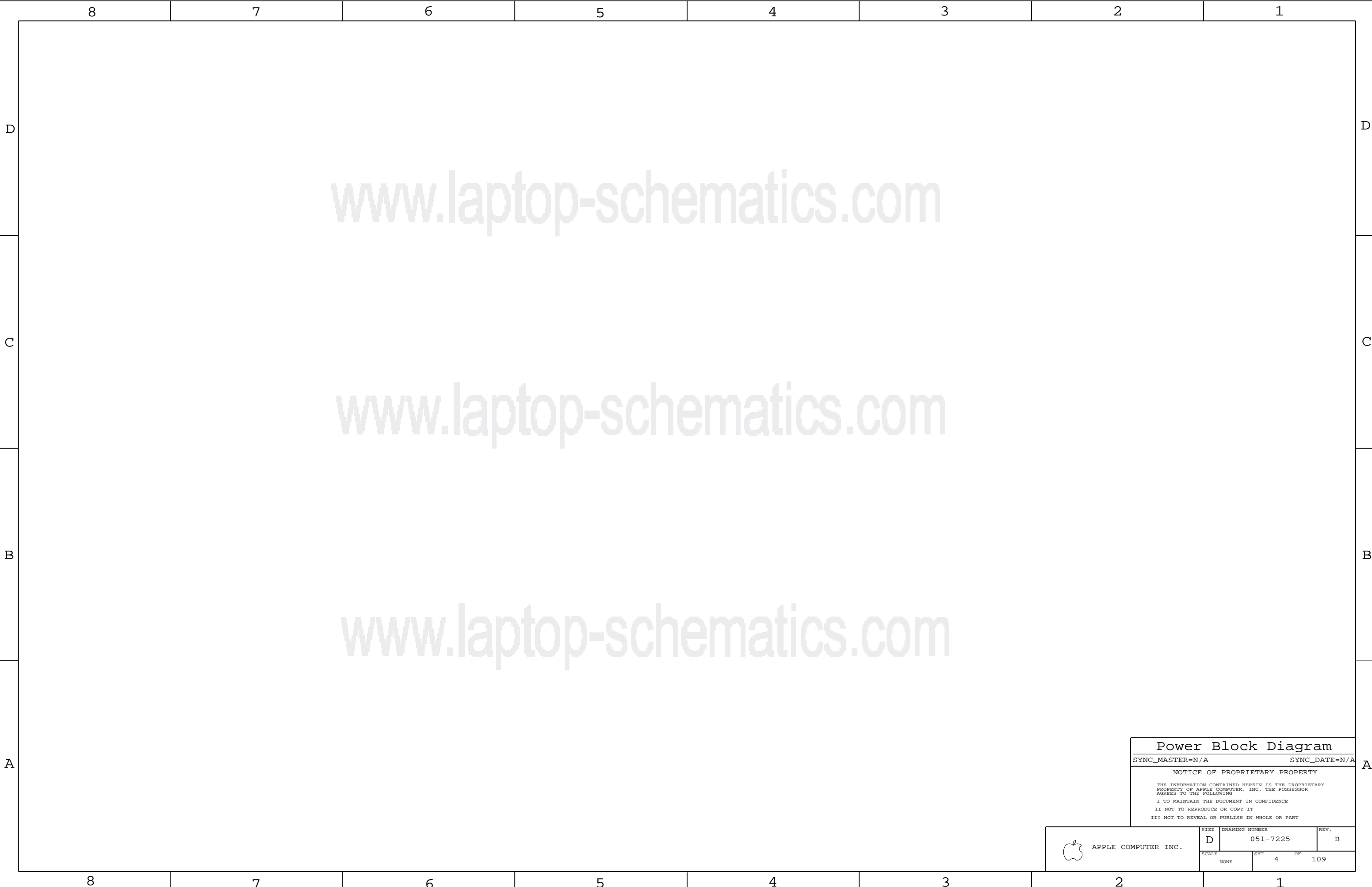
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Power Block Diagram		
SYNC_MASTER=(T9_MLB)		SYNC_DATE=08/23/2006
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Power Block Diagram

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## BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA, 2.2GHZ, 128SAM_VRAM,M75,MBP15	M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG
630-7932	PCBA, 2.4GHZ, 256SAM_VRAM,M75,MBP15	M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG
630-8659	PCBA, 2.2GHZ, 128HY_VRAM,M75,MBP15	M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX
630-8662	PCBA, 2.4GHZ, 256HY_VRAM,M75,MBP15	M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX

## M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	PIV8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128, VRAM_SAMSUNG, VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128, VRAM_HYNIX, VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

## Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3464	1	IC,MDC,SR,E1,PRQ,2.2Q,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3465	1	IC,MDC,SR,E1,PRQ,2.4Q,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,1F	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,1W PWR CLKCK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,H58/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	1C,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	1C,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	1C,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	1C,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15780011	15780030		ALL	MR alt to 15780011-Push negative
15280476	15280276		ALL	Inductor alternate
35331681	35331294		ALL	TV alt to National
13880603	13880602		ALL	Murata alt to Samsung

## BOM Configuration

SYNC_MASTER=N/A	SYNC_DATE=N/A
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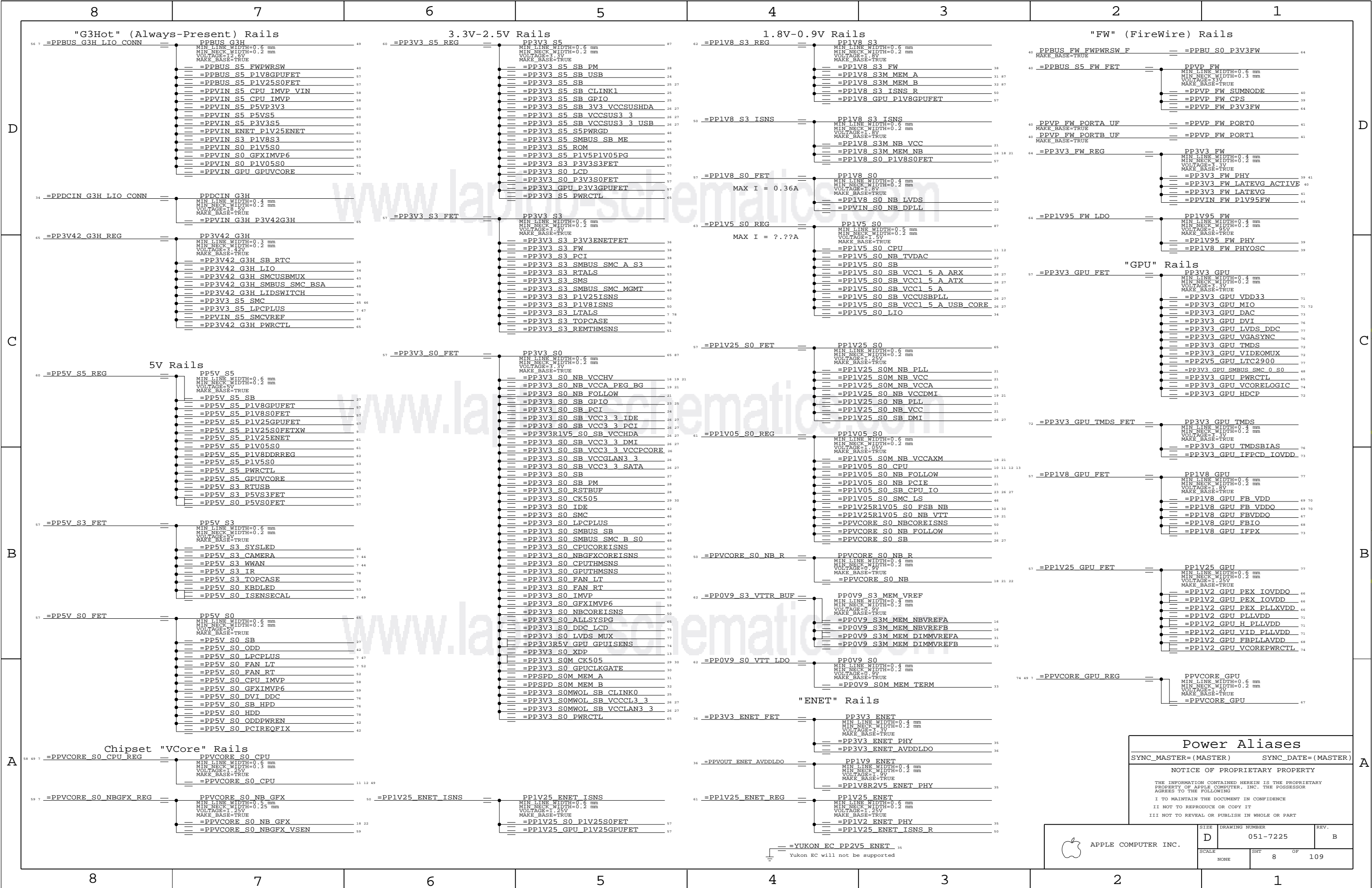
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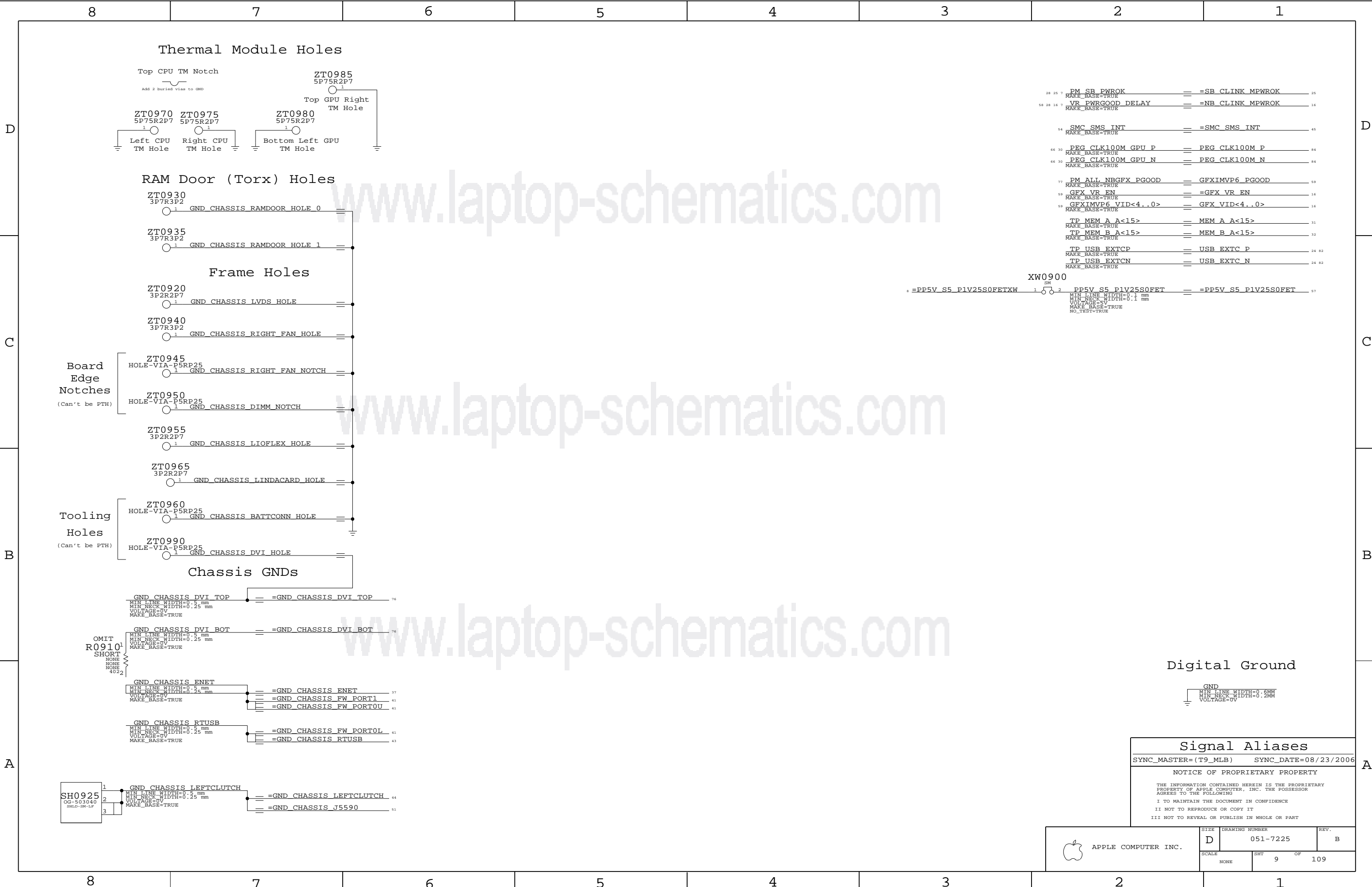




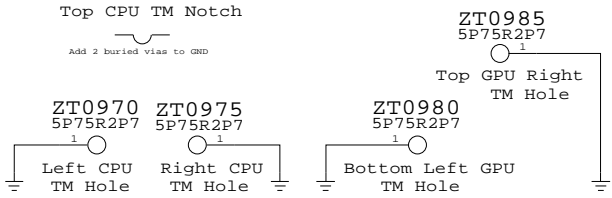




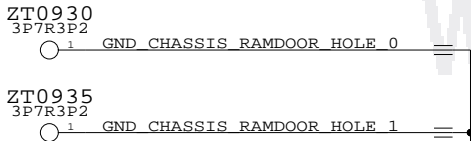




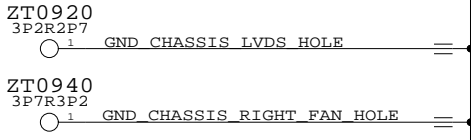
Thermal Module Holes



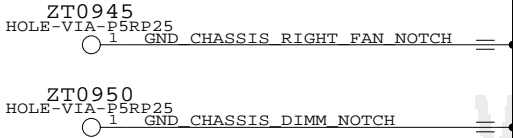
RAM Door (Torx) Holes



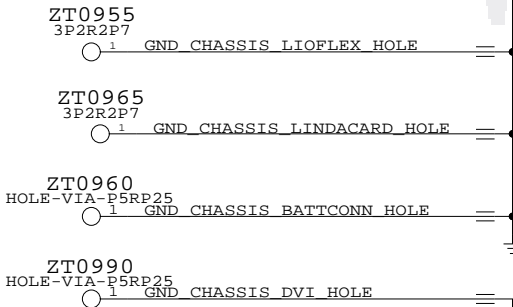
Frame Holes



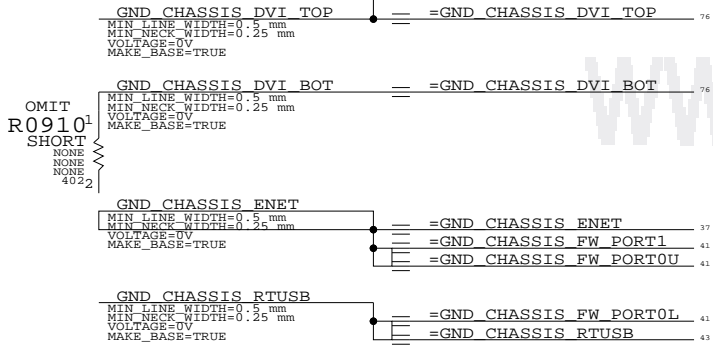
Board Edge Notches  
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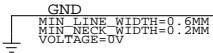
Tooling Holes  
(Can't be PTH)



Chassis GNDs



Digital Ground



Signal Aliases

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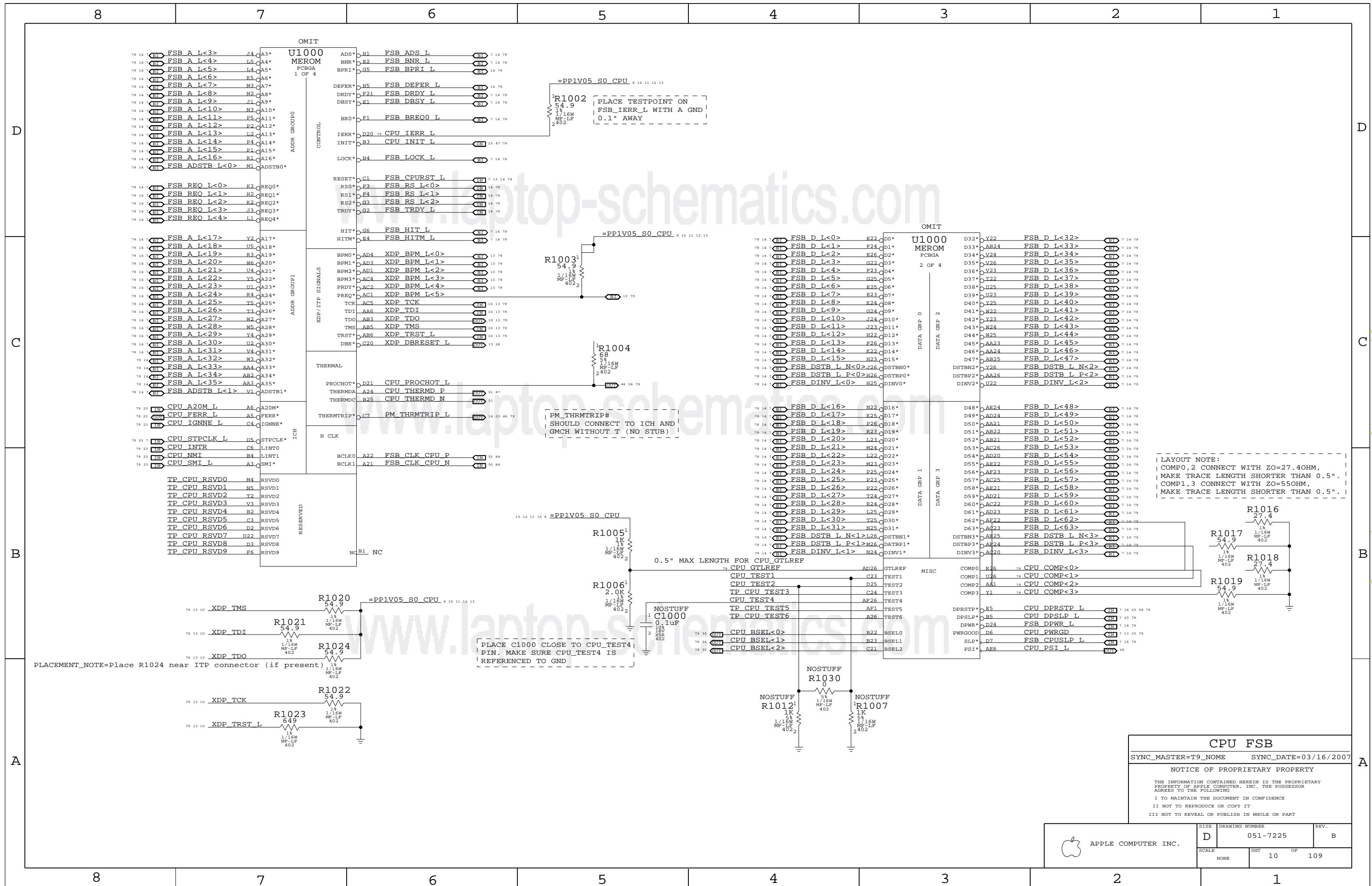
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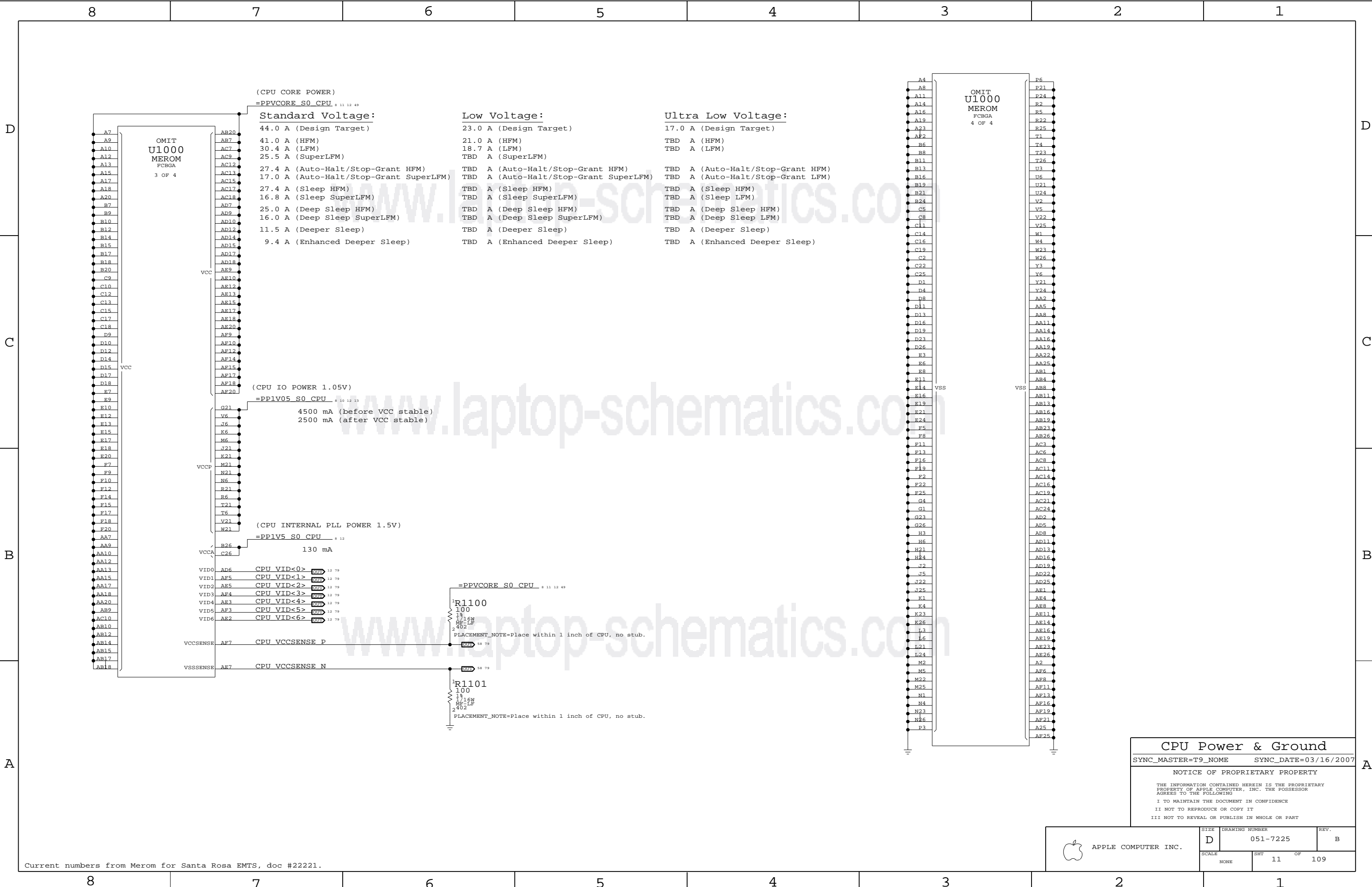
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(CPU CORE POWER)

=PPVCORE\_S0\_CPU\_8 11 12 49

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

OMIT  
U1000  
MEROM  
FCBGA  
3 OF 4

OMIT  
U1000  
MEROM  
FCBGA  
4 OF 4

CPU Power & Ground

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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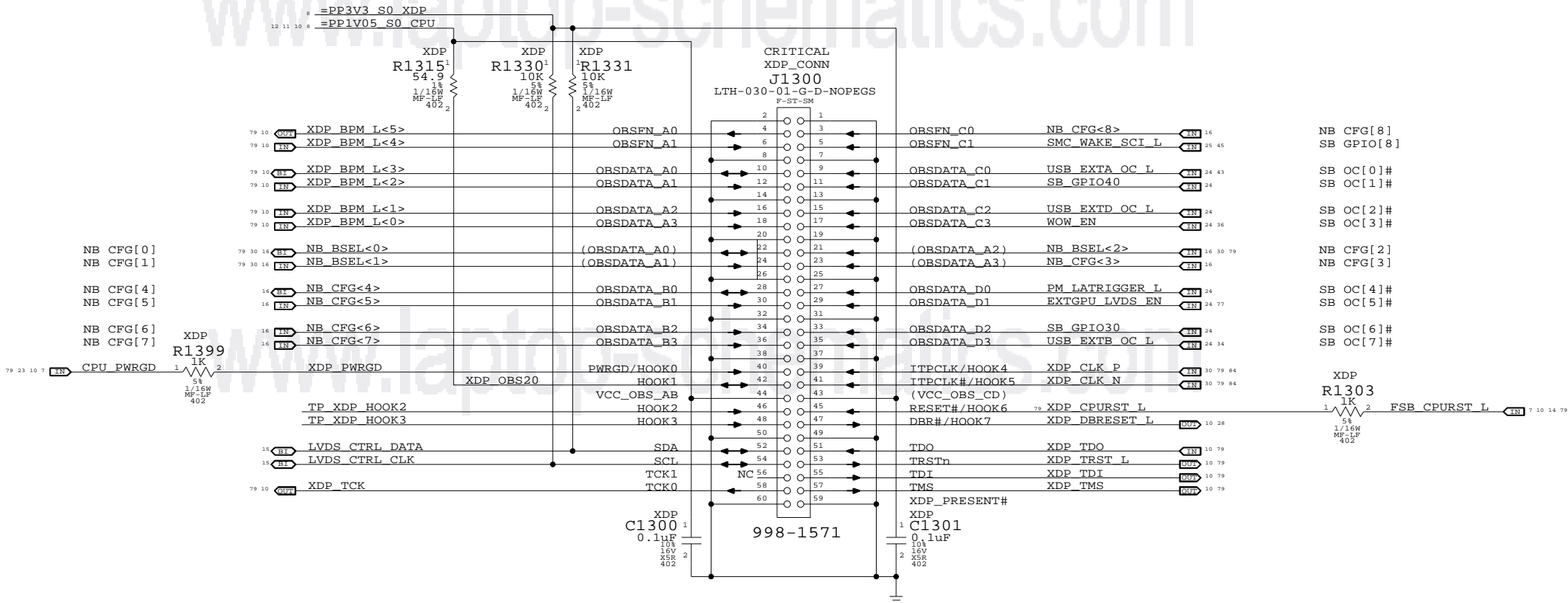
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B

A

# Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions  
on even-numbered side of J1300

## eXtended Debug Port (XDP)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=12/12/2006

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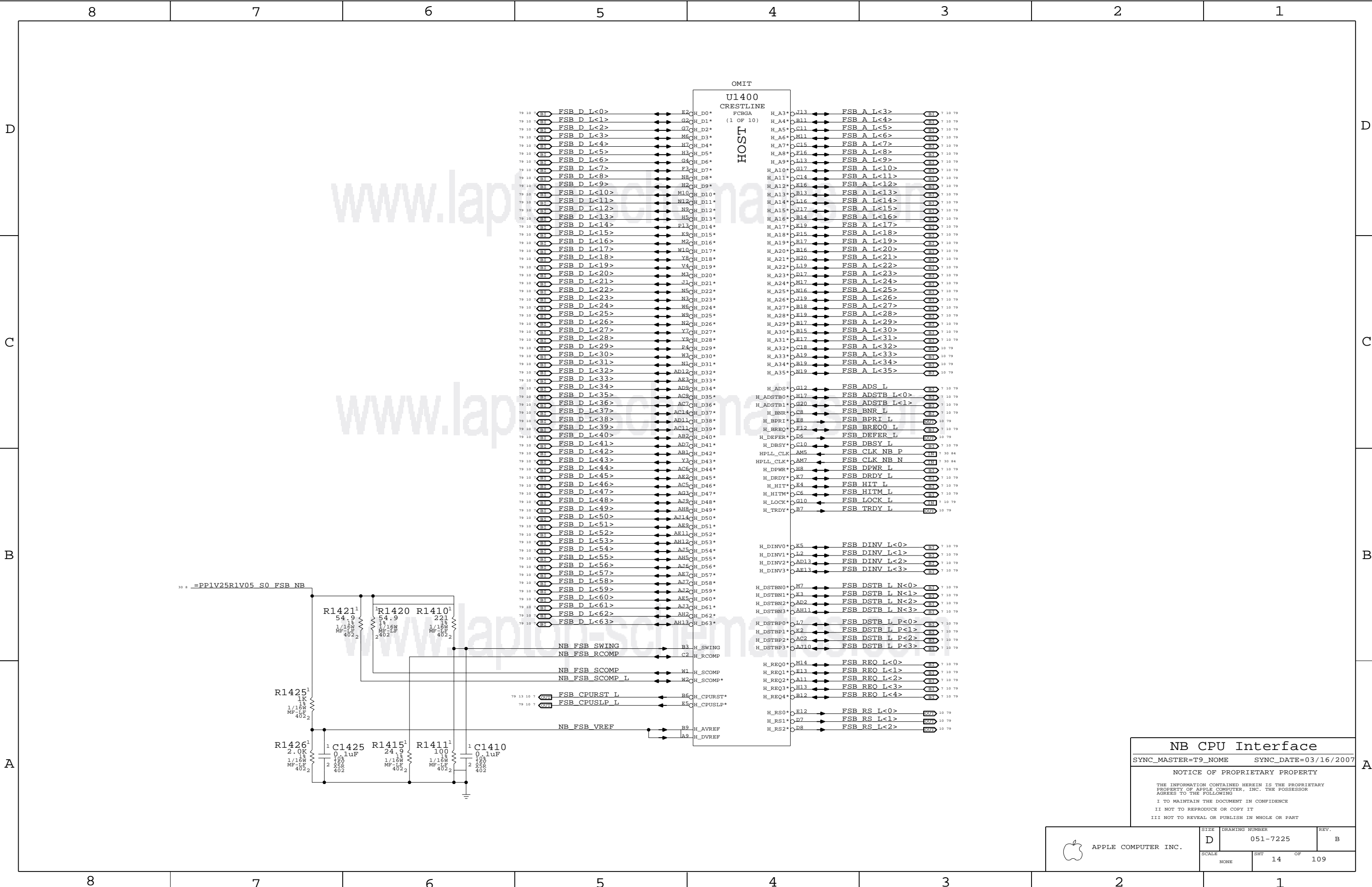
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NB CPU Interface

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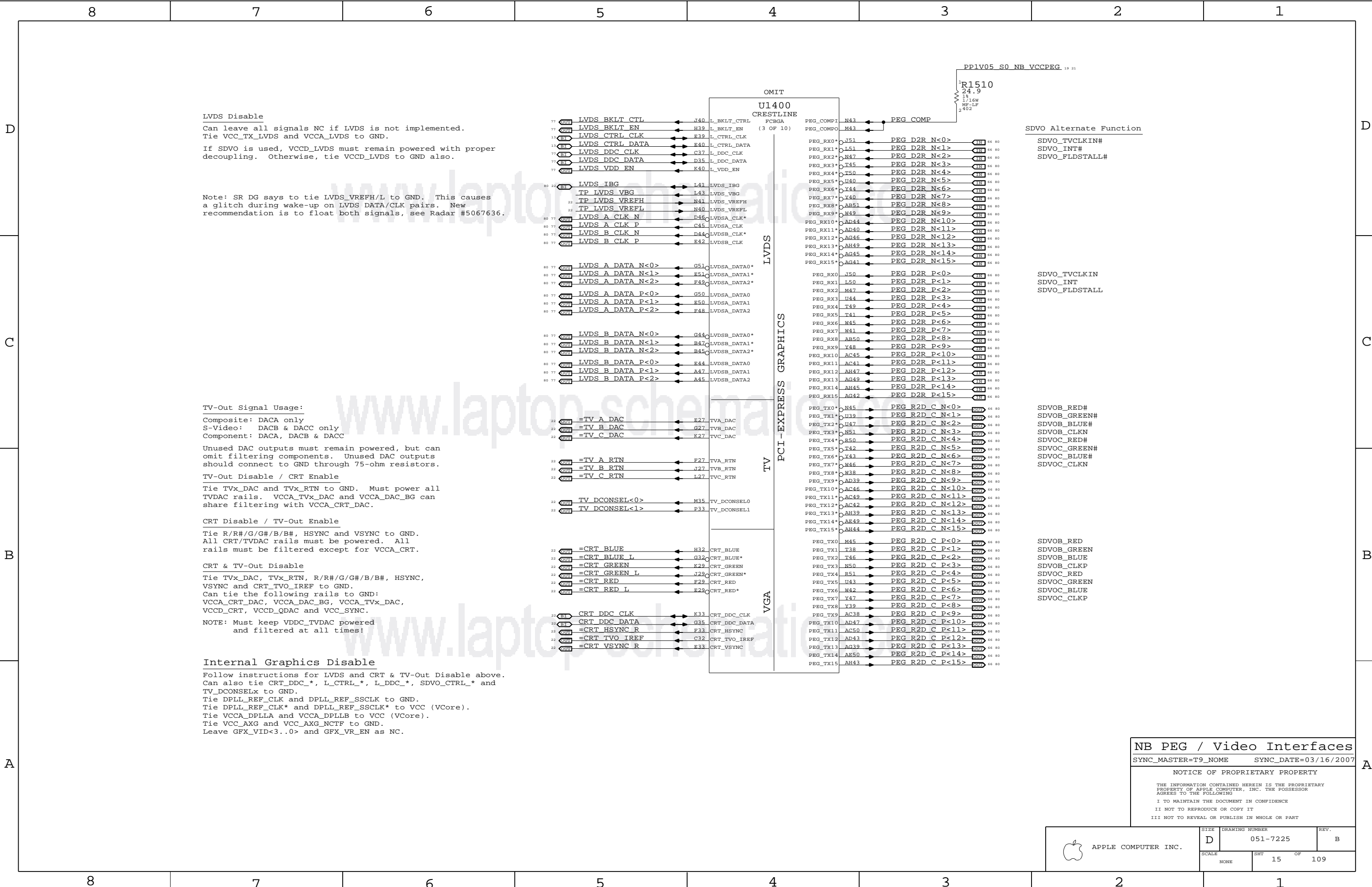
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NB PEG / Video Interfaces

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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SIZE

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DRAWING NUMBER

051-7225

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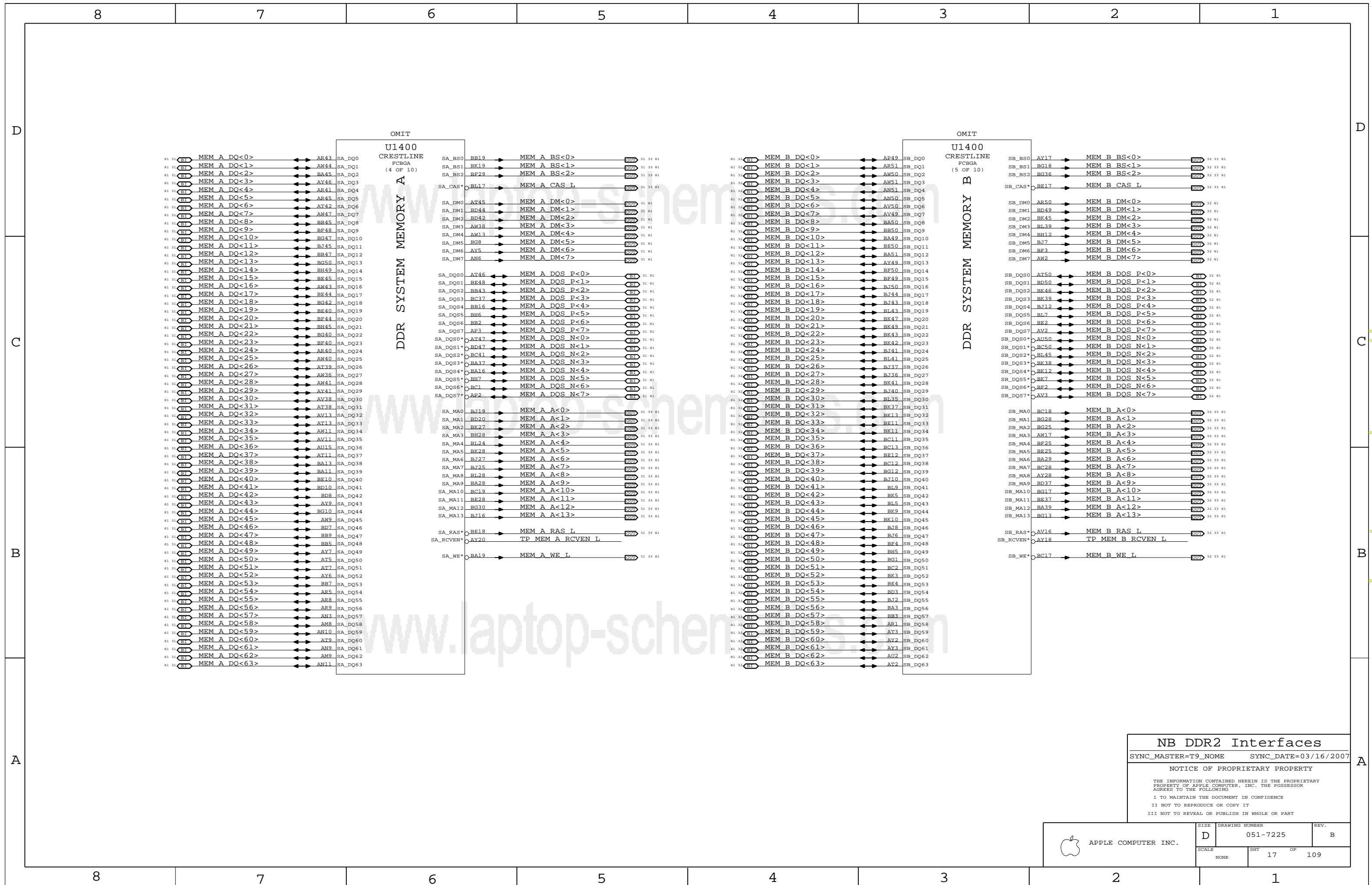
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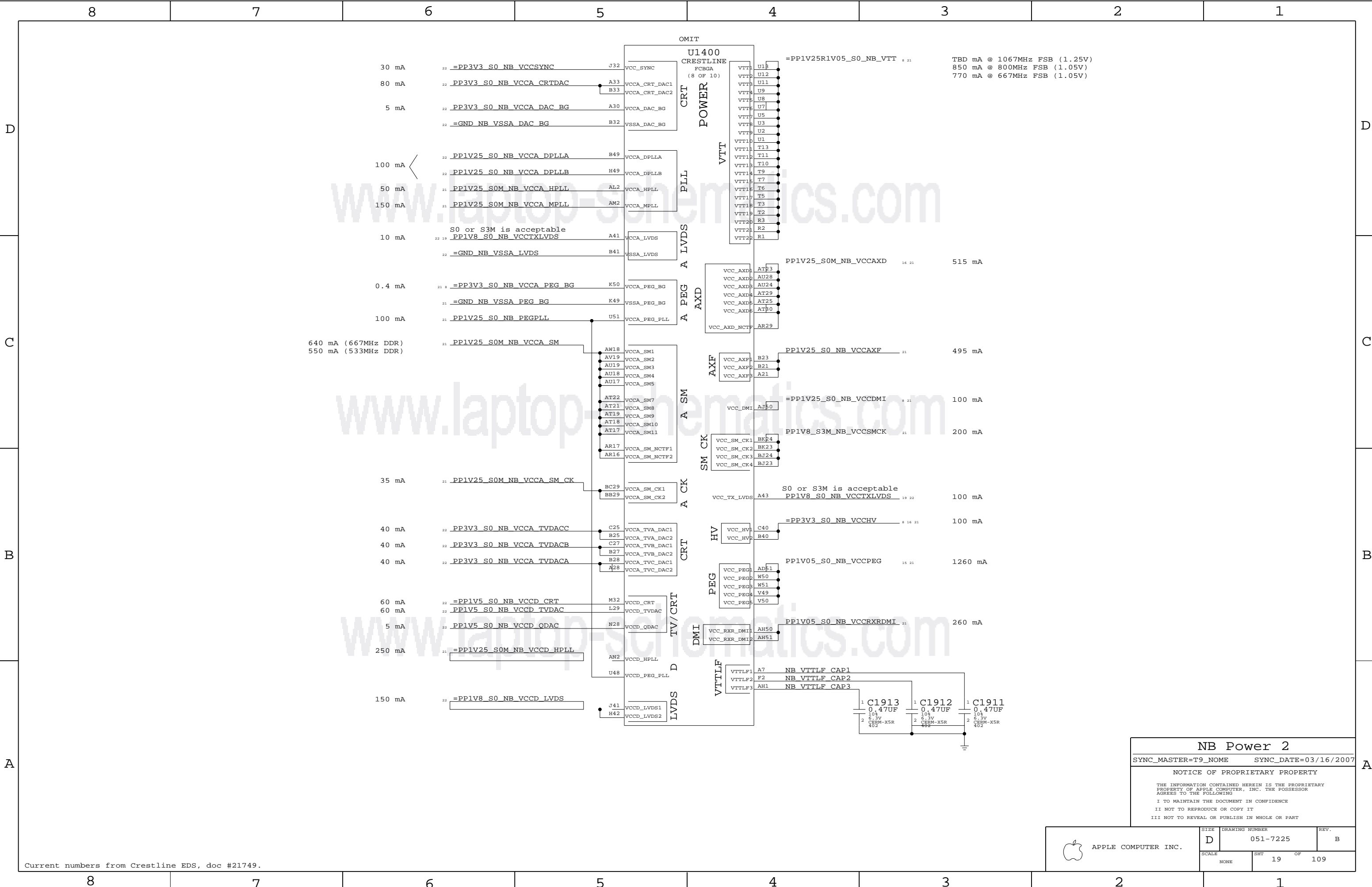












NB Power 2

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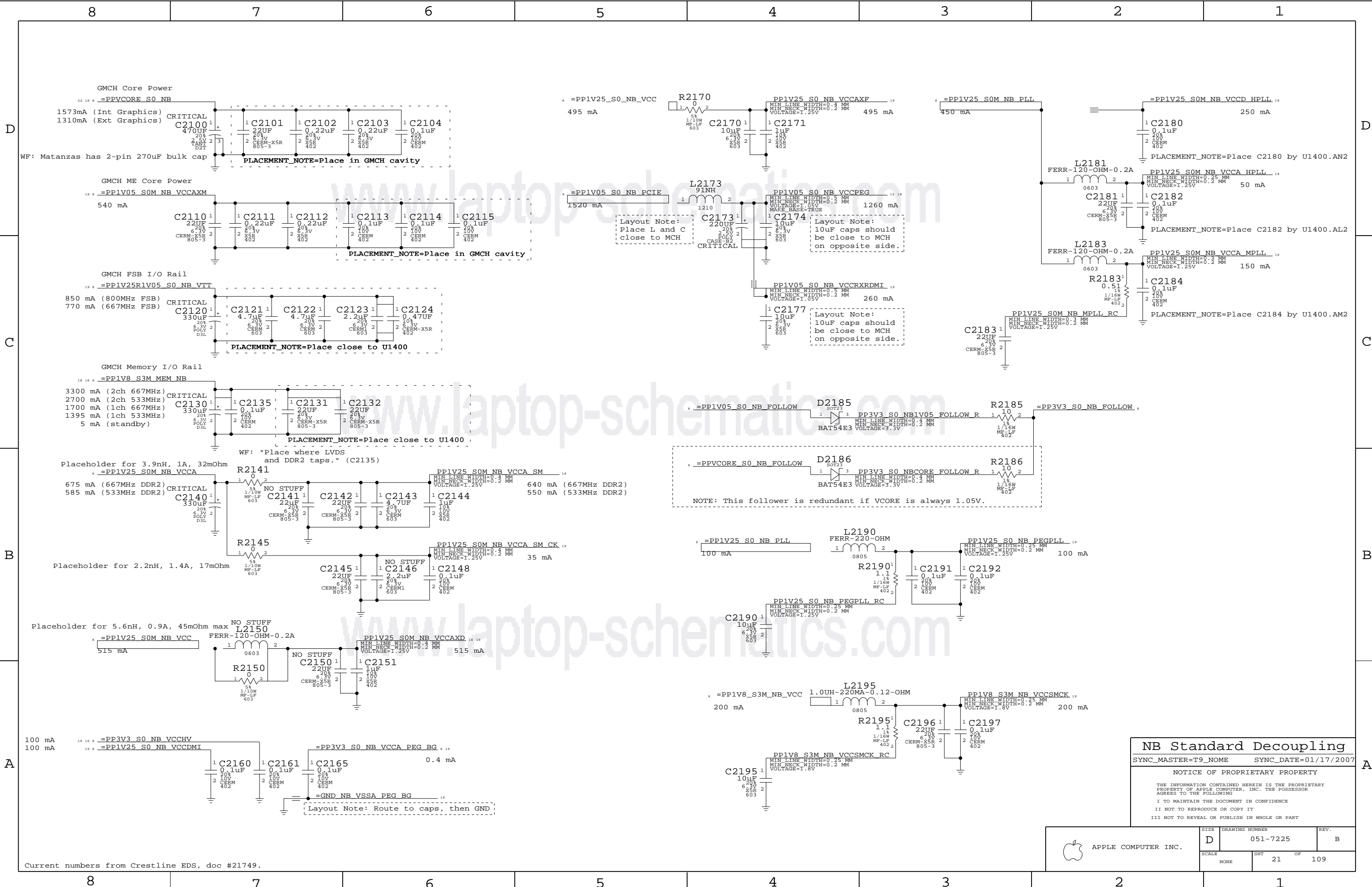
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	D	051-7225	B
SCALE		SHT	OF
NONE		19	109



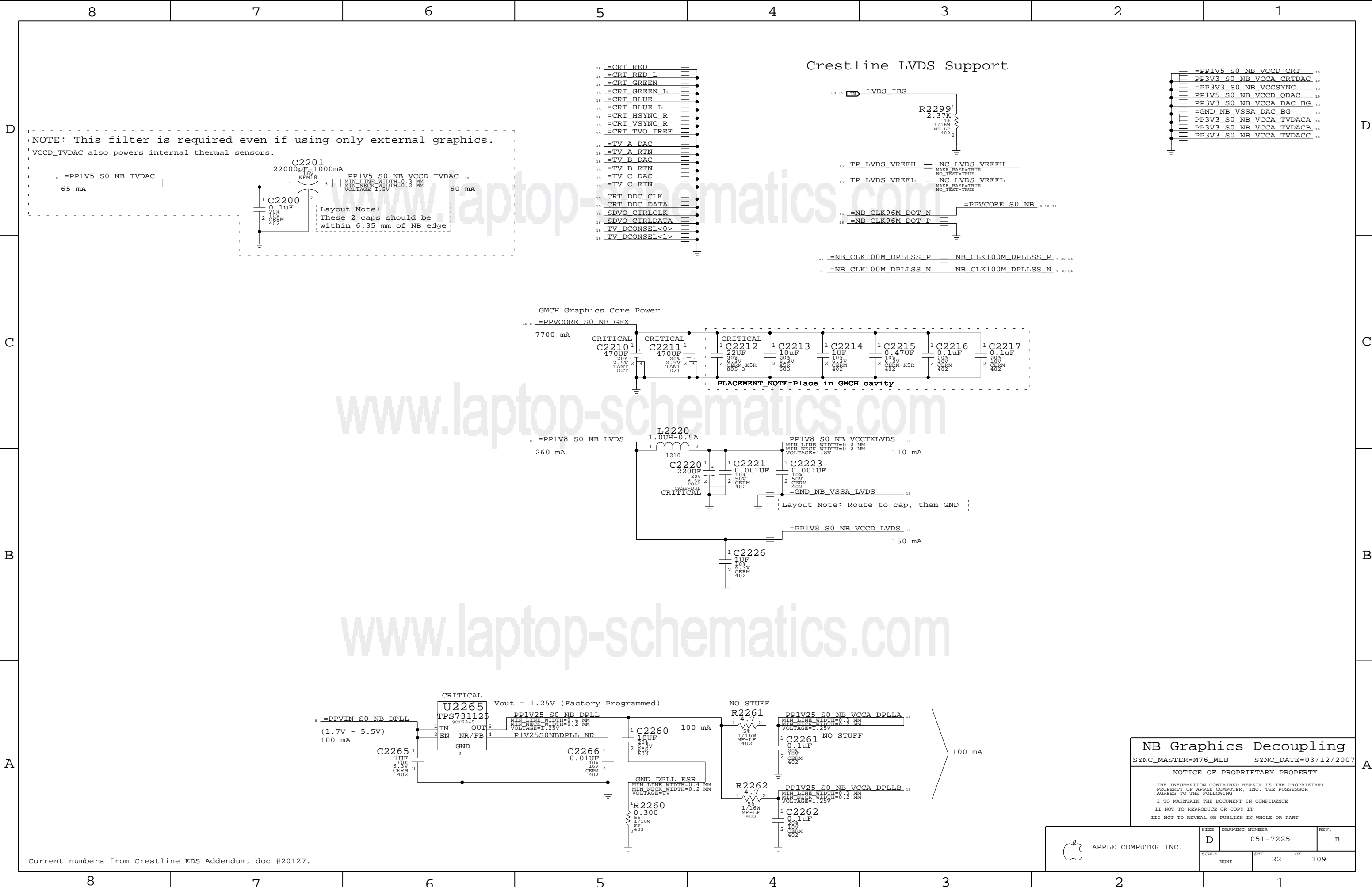


### NB Standard Decoupling

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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	D	051-7225	B
SCALE	SHT		
	21 OF 109		



NOTE: This filter is required even if using only external graphics.  
VCCD\_TVDAC also powers internal thermal sensors.

=PP1V5\_S0\_NB\_TVDAC  
65 mA

C2201  
22000pF-1000mA  
16V  
NFM18  
MIN LINE WIDTH=0.3 MM  
MIN NECK WIDTH=0.2 MM  
VOLTAGE=1.5V

PP1V5\_S0\_NB\_VCCD\_TVDAC  
60 mA

Layout Note:  
These 2 caps should be  
within 6.35 mm of NB edge

GMCH Graphics Core Power

=PPVCORE\_S0\_NB\_GFX  
7700 mA

CRITICAL C2210 470UF  
CRITICAL C2211 470UF  
CRITICAL C2212 22UF  
C2213 10uF  
C2214 1uF  
C2215 0.47UF  
C2216 0.1uF  
C2217 0.1uF

PLACEMENT NOTE=Place in GMCH cavity

=PP1V8\_S0\_NB\_LVDS  
260 mA

L2220 1.00H-0.5A  
1210

CRITICAL C2220 220UF  
C2221 0.001UF  
C2222 0.001UF  
C2223 0.001UF  
C2226 1UF

PP1V8\_S0\_NB\_VCCTXLVDS  
110 mA

PP1V8\_S0\_NB\_VCCD\_LVDS  
150 mA

Layout Note: Route to cap, then GND

CRITICAL U2265  
TPS731125  
SOT23-5  
Vout = 1.25V (Factory Programmed)

=PPVIN\_S0\_NB\_DPLL  
(1.7V - 5.5V)  
100 mA

C2265 1UF  
C2266 0.01UF  
C2260 10UF  
C2261 0.1uF  
C2262 0.1uF

R2260 0.300  
R2261 1/16W  
R2262 1/16W

PP1V25\_S0\_NB\_DPLL  
100 mA

PP1V25\_S0\_NB\_VCCA\_DPLLA  
100 mA

PP1V25\_S0\_NB\_VCCA\_DPLLB  
100 mA

Crestline LVDS Support

=PP1V5\_S0\_NB\_VCCD\_CRT  
PP3V3\_S0\_NB\_VCCA\_CRTDAC  
PP3V3\_S0\_NB\_VCCSYNC  
PP1V5\_S0\_NB\_VCCD\_ODAC  
PP3V3\_S0\_NB\_VCCA\_DAC\_BG  
PP3V3\_S0\_NB\_VCCA\_TVDACA  
PP3V3\_S0\_NB\_VCCA\_TVDACB  
PP3V3\_S0\_NB\_VCCA\_TVDACC

NB Graphics Decoupling

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007

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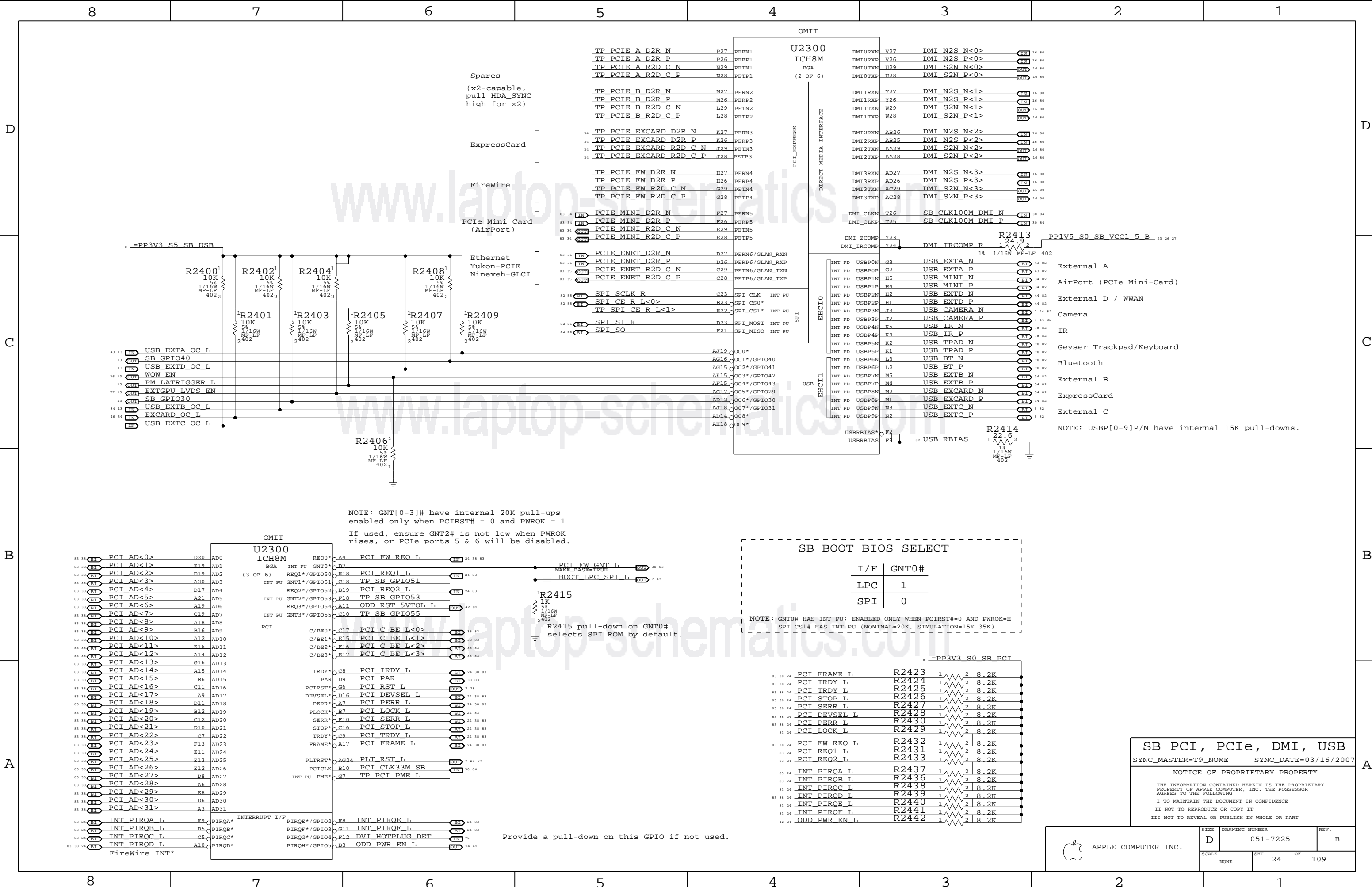
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. B

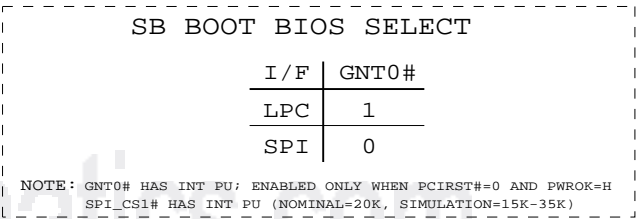
SCALE NONE SHT 22 OF 109







NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1  
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.



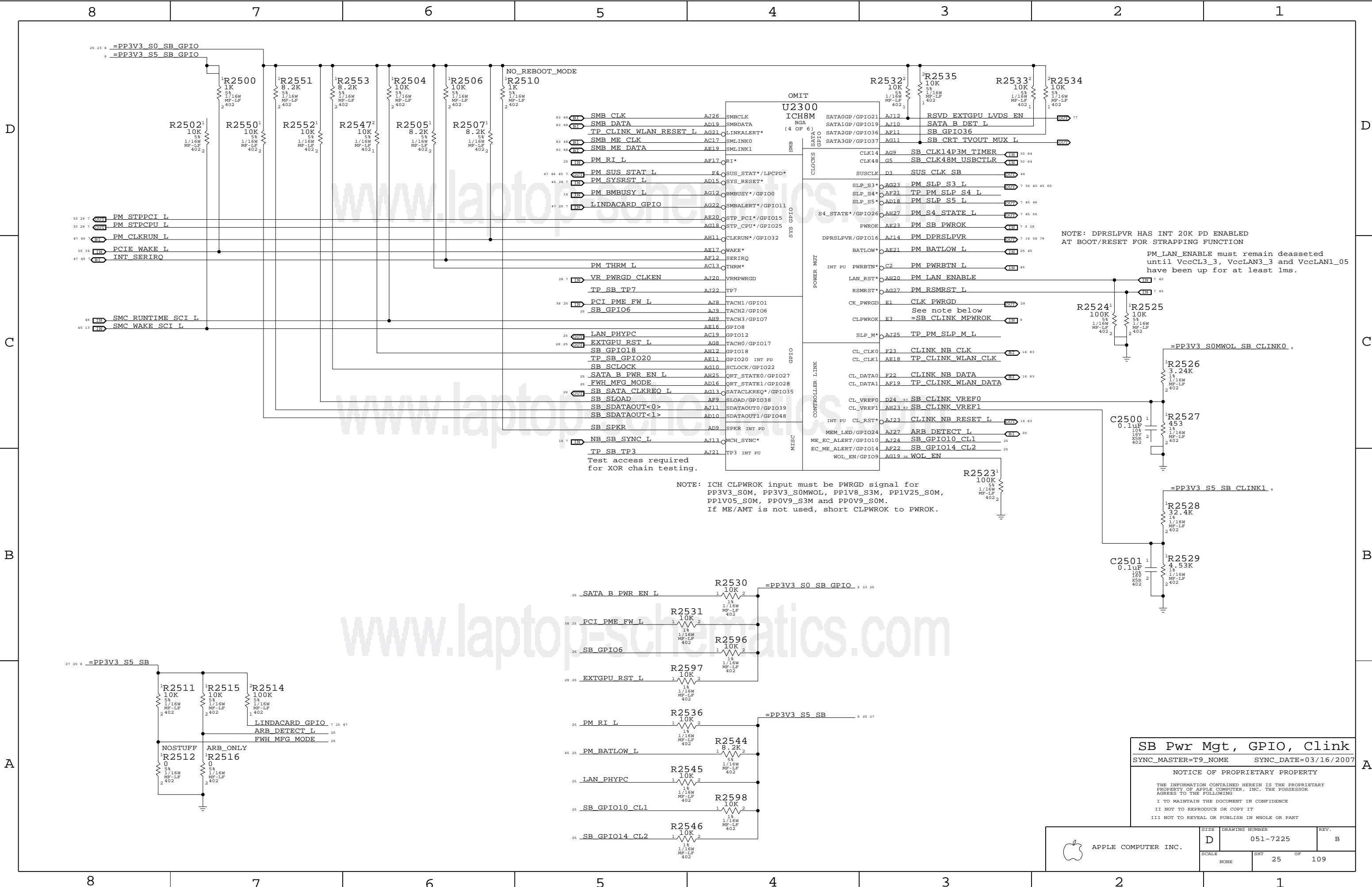
SB PCI, PCIe, DMI, USB

SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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U2300 ICH8M (4 OF 6)		
82 48	SMB CLK	AJ26 SMBCLK
82 48	SMB DATA	AD19 SMBDATA
82 48	TP CLINK WLAN RESET L	AG21 LINKALERT*
82 48	SMB ME CLK	AC17 SMLINK0
82 48	SMB ME DATA	AE19 SMLINK1
25	PM RI L	AF17 RI*
47 46 45 7	PM SUS_STAT L	F4 SUS_STAT*/LPCPD*
45 28 7	PM_SYSRST L	AD15 SYS_RESET*
16	PM_BMBUSY L	AG12 BMBUSY*/GPIO0
47 25 7	LINDACARD GPIO	AG22 SMBALERT*/GPIO11
		AE20 STP_PCI*/GPIO15
		AG18 STP_CPU*/GPIO25
		AH11 CLKRUN*/GPIO32
		AE17 WAKE*
		AF12 SERIRQ
		AC13 THRM*
28 7	VR_PWRGD CLKEN	AJ20 VRMPWRGD
		AJ22 TP7
38 25	PCI PME FW L	AT8 TACH1/GPIO1
		AT9 TACH2/GPIO6
		AH9 TACH3/GPIO7
		AE16 GPIO8
25	LAN PHYPC	AC19 GPIO12
28 25	EXTGPU_RST L	AG8 TACH0/GPIO17
		AH12 GPIO18
		AE11 GPIO20 INT PD
		AG10 SCLOCK/GPIO22
25	SATA_B_PWR_EN L	AH25 QRT_STATE0/GPIO27
25	FWH_MFG_MODE	AD16 QRT_STATE1/GPIO28
29	SB_SATA_CLKREQ L	AG13 SATACLKREQ*/GPIO35
		AE9 SLOAD/GPIO38
		AJ11 SDATAOUT0/GPIO39
		AD10 SDATAOUT1/GPIO48
		AD9 SPKR INT PD
16 7	NB_SB_SYNC L	AJ13 MCH_SYNC*
		AJ21 TP3 INT PU

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PP0V9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION. PM\_LAN\_ENABLE must remain deasserted until VccCL3\_3, VccLAN3\_3 and VccLAN1\_05 have been up for at least 1ms.

SB Pwr Mgt, GPIO, Clink  
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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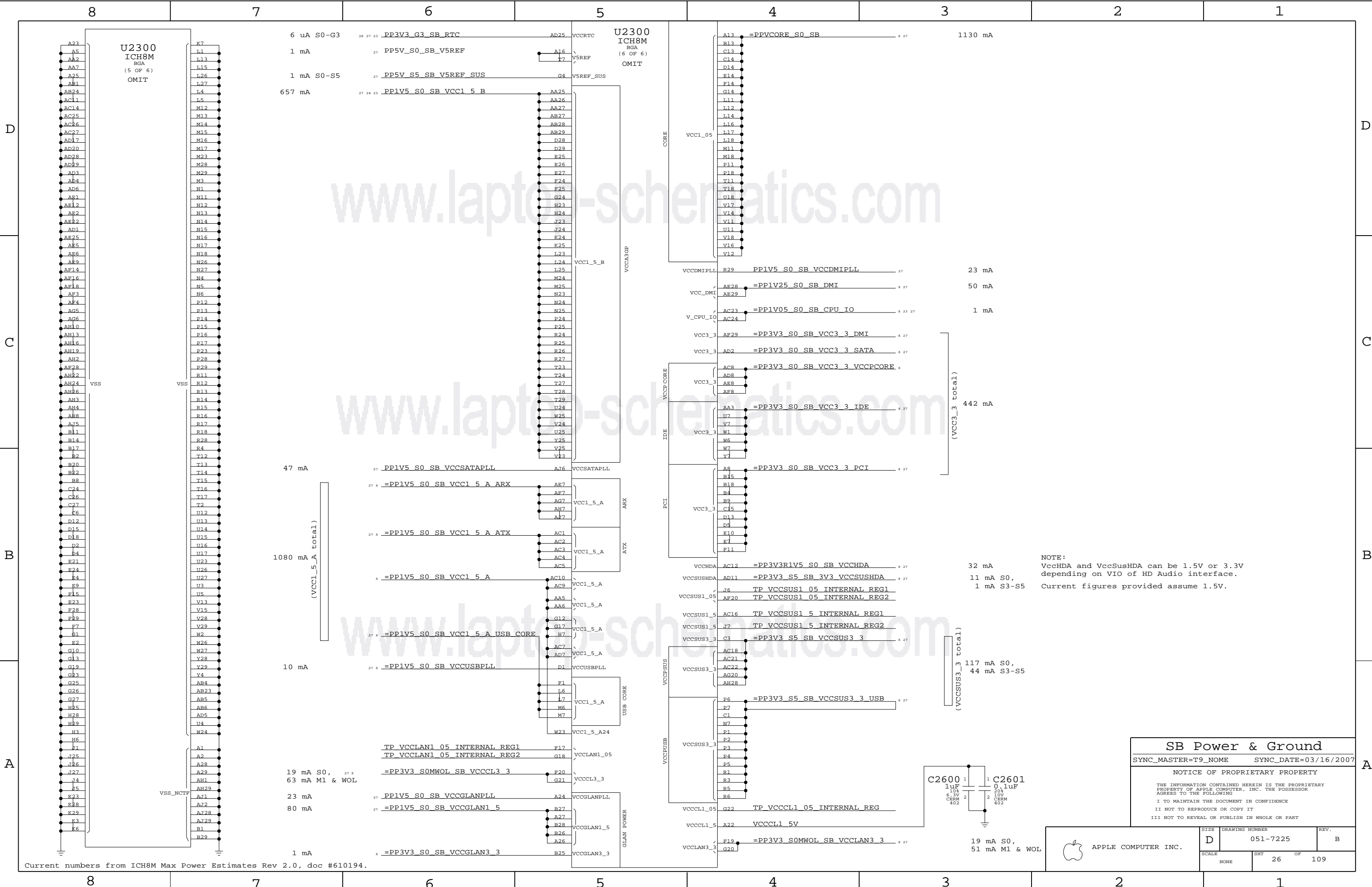
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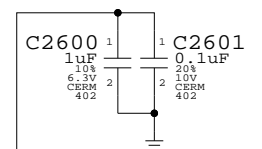
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NONE		25	109



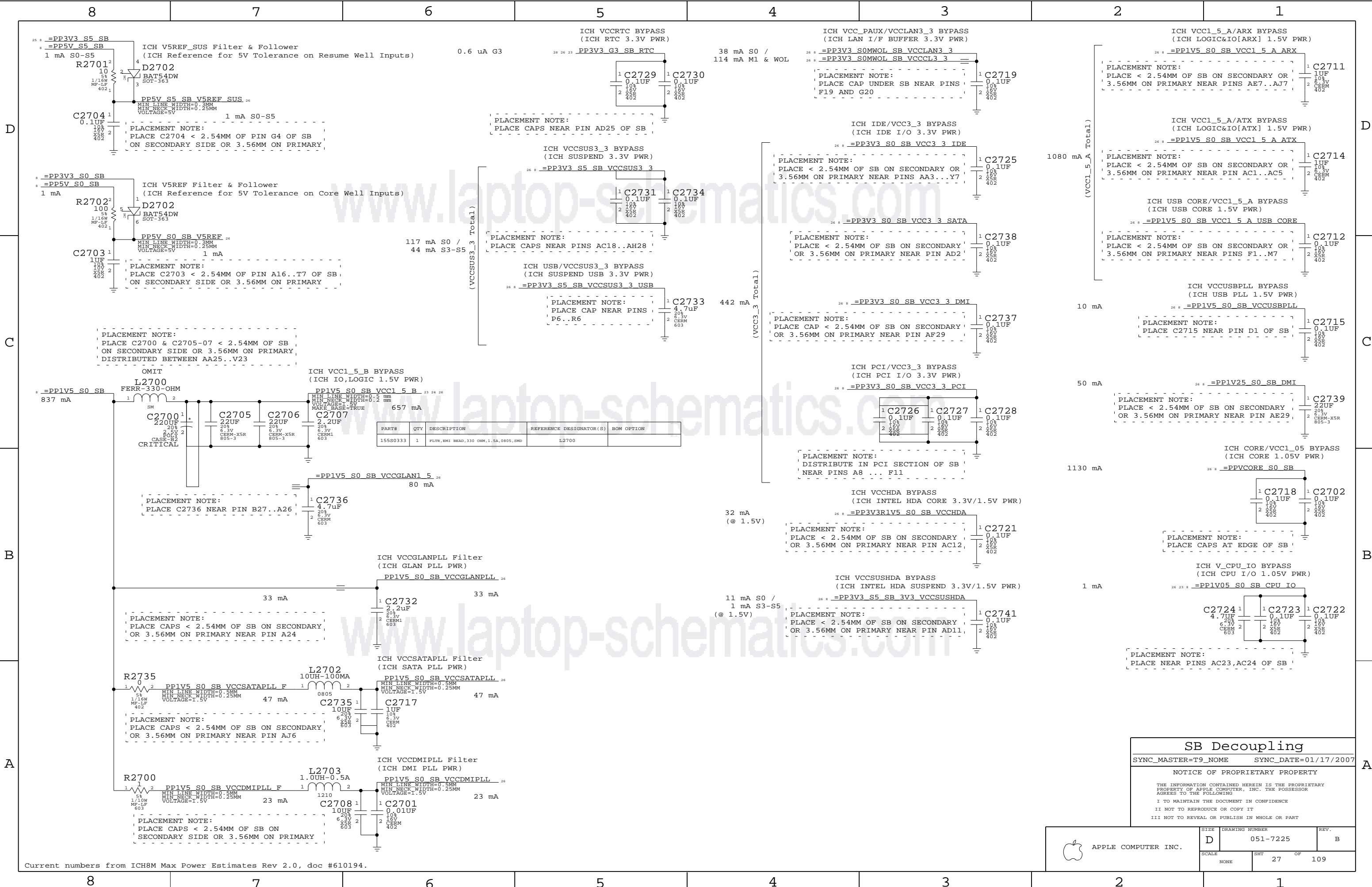
NOTE:  
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
Current figures provided assume 1.5V.



SB Power & Ground		
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NONE		26	109

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.



SB Decoupling

SYNC\_MASTER=T9\_NOME

SYNC\_DATE=01/17/2007

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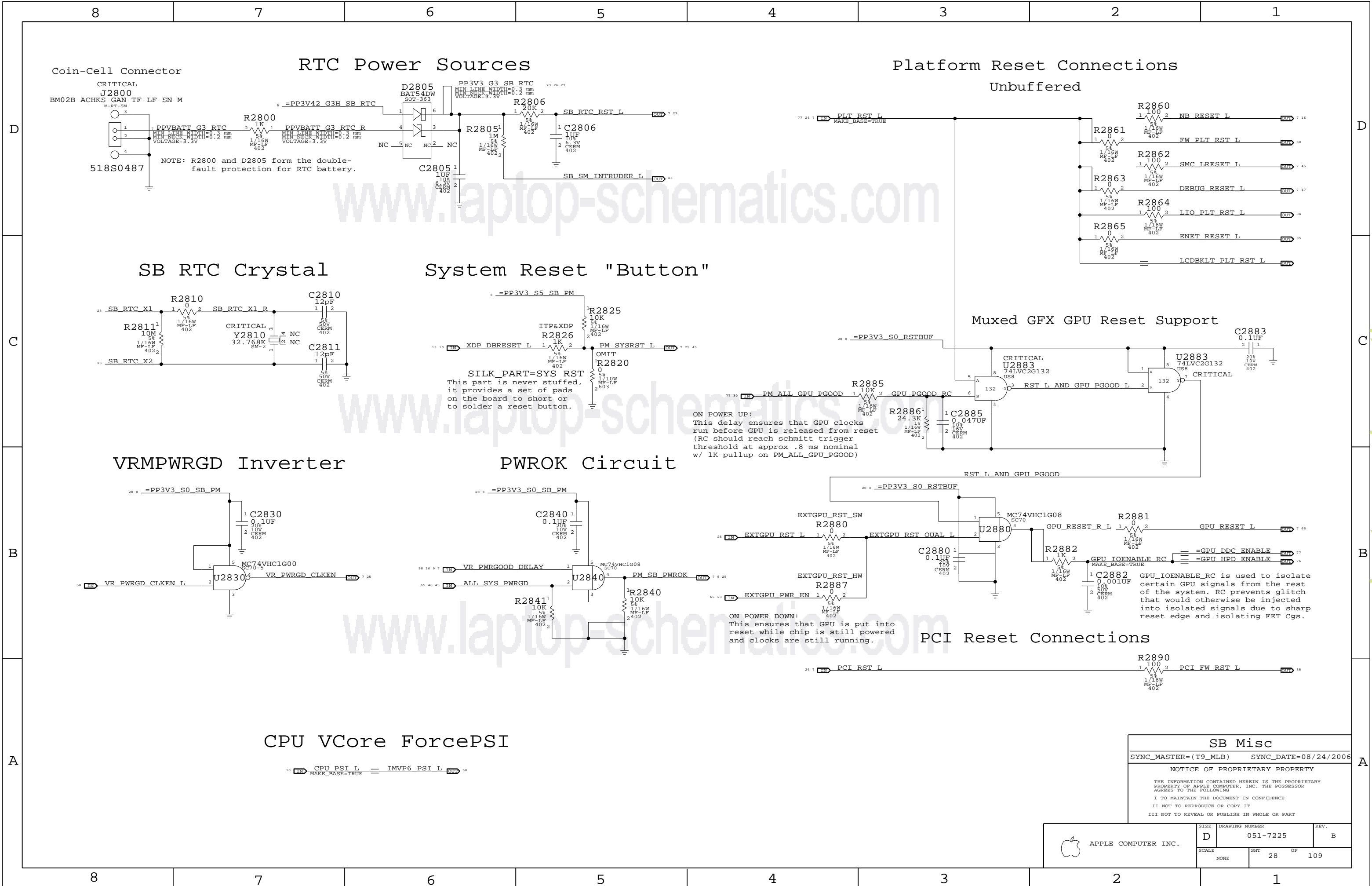
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SCALE		SHT	OF
NONE		27	109





D

C

B

A

D

C

B

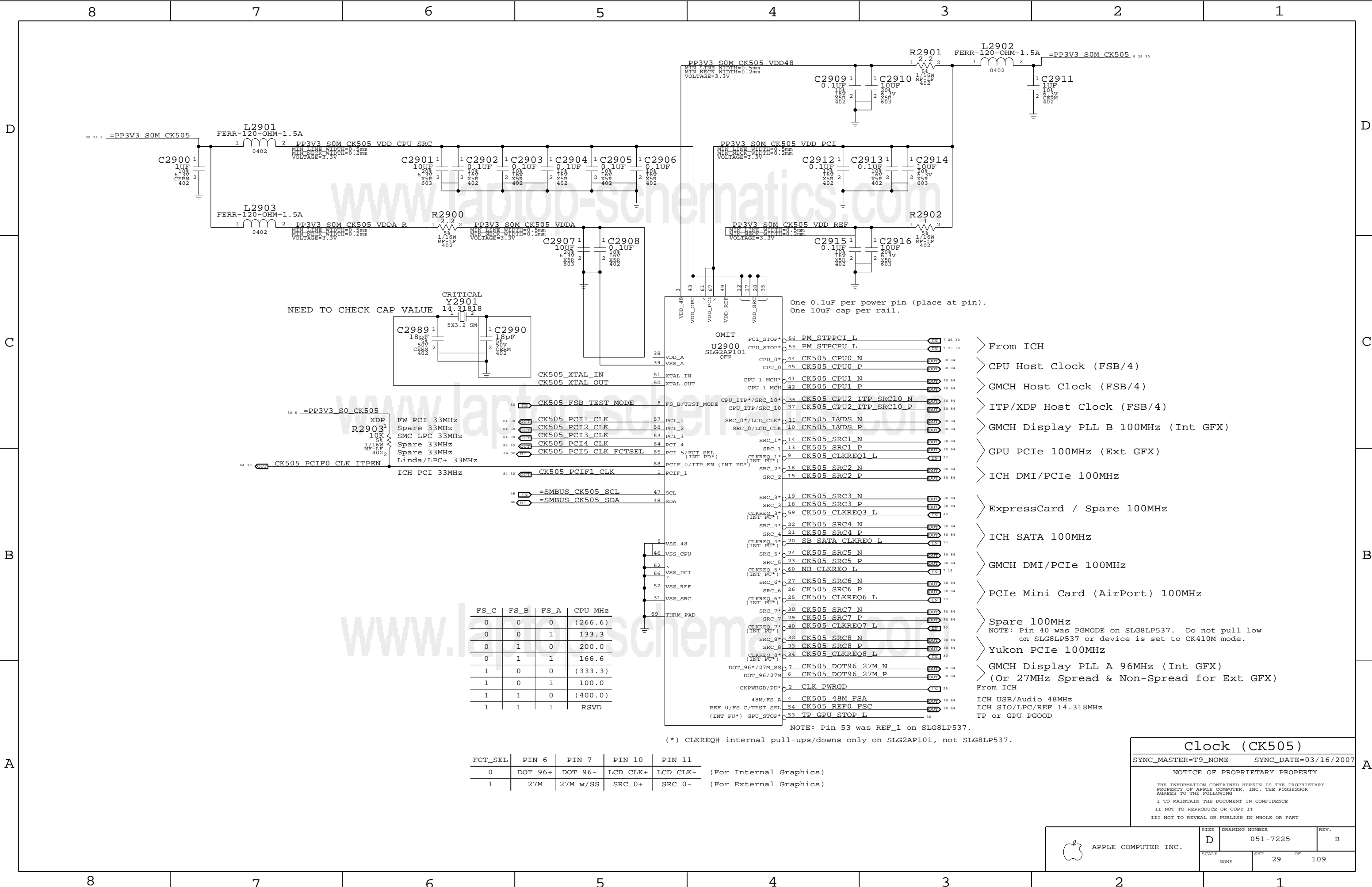
A

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SB Misc		
SYNC_MASTER=(T9_MLB)		SYNC_DATE=08/24/2006
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SCALE		SHT	OF
NONE		28	109





D

C

B

A

D

C

B

A

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FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)  
(For External Graphics)

Clock (CK505)

SYNC\_MASTER=T9\_NOME    SYNC\_DATE=03/16/2007

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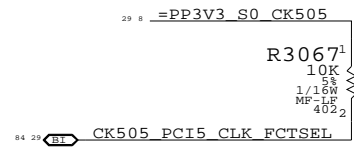
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SIZE D    DRAWING NUMBER 051-7225    REV. B

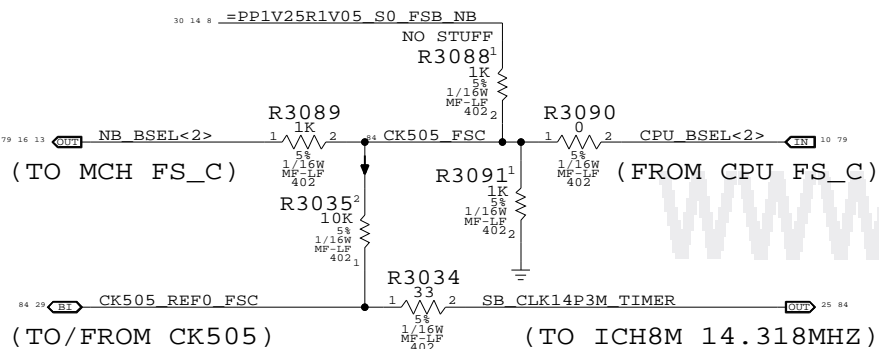
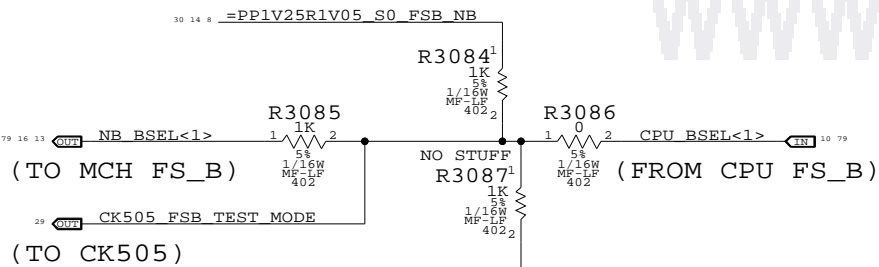
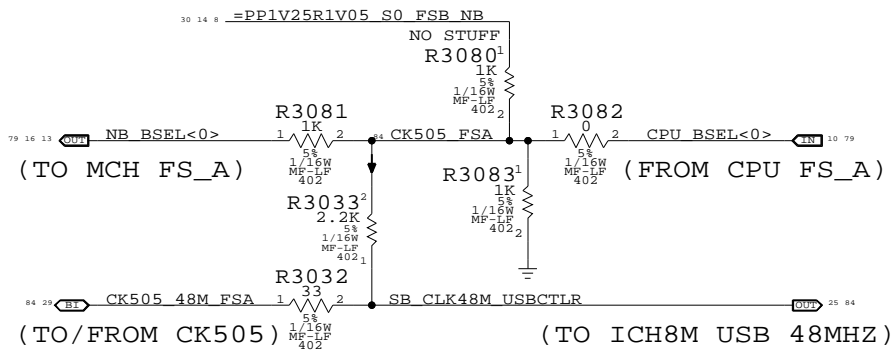
SCALE NONE    SHT 29 OF 109

## CK505 Configuration Straps

FCT\_SEL (GFX clock select)



FS\_A, FS\_B, FS\_C (Host clock freq select)



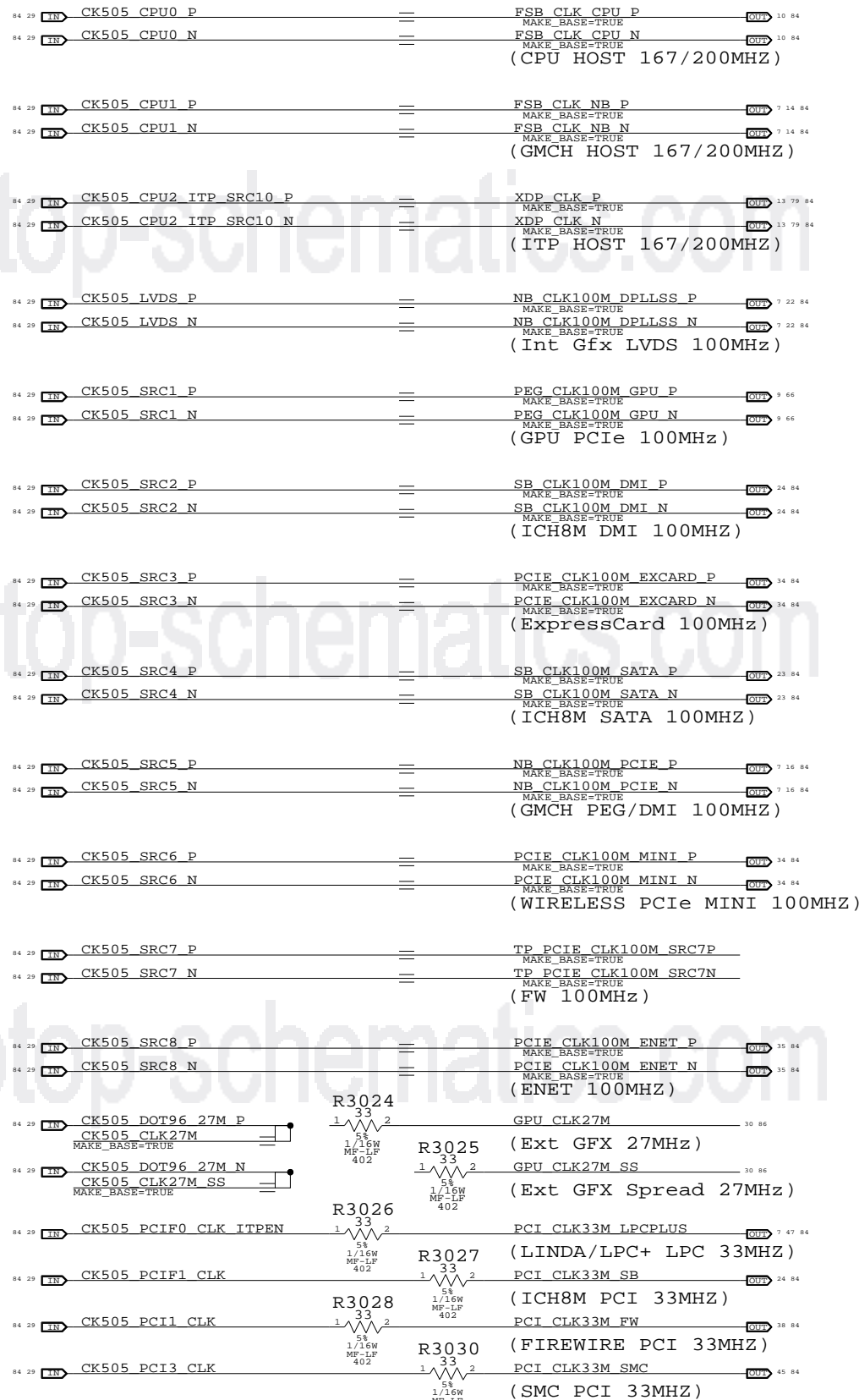
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

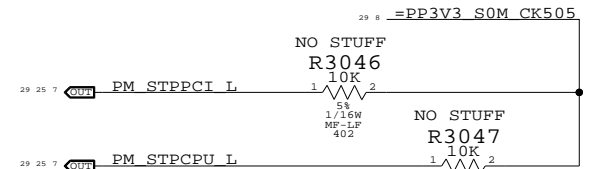
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

## CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)

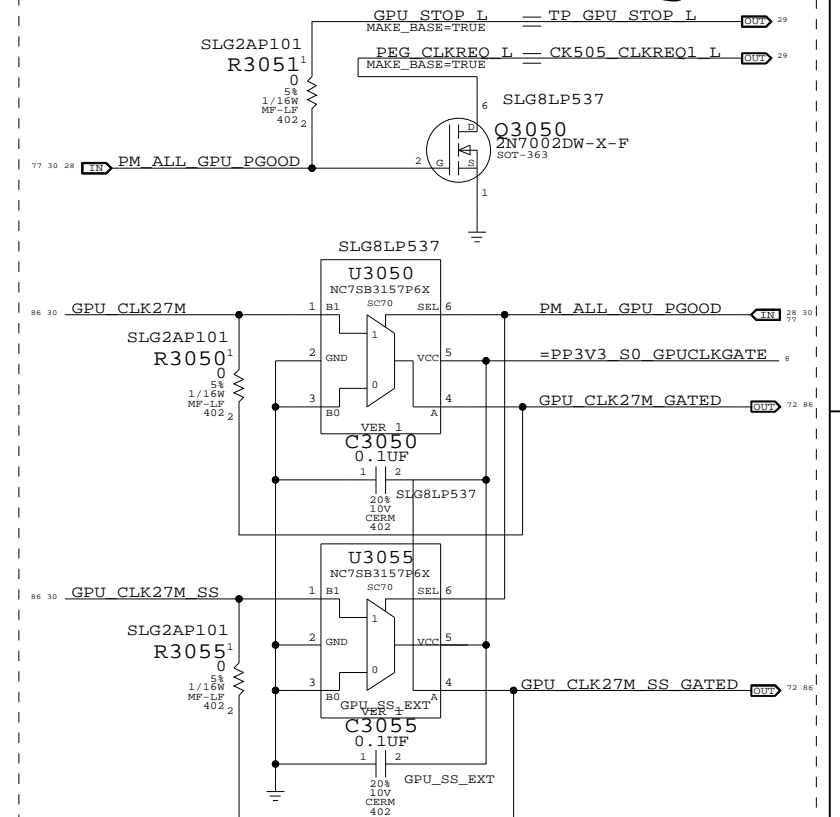


## CLKREQ Controls

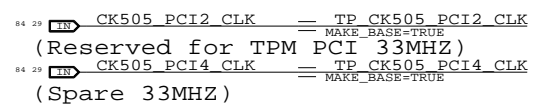


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

## GPU Clock Gating



## Unused Clocks



## Clock Termination

SYNC\_MASTER=(MASTER) SYNC\_DATE=08/23/2006

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NONE	30	109

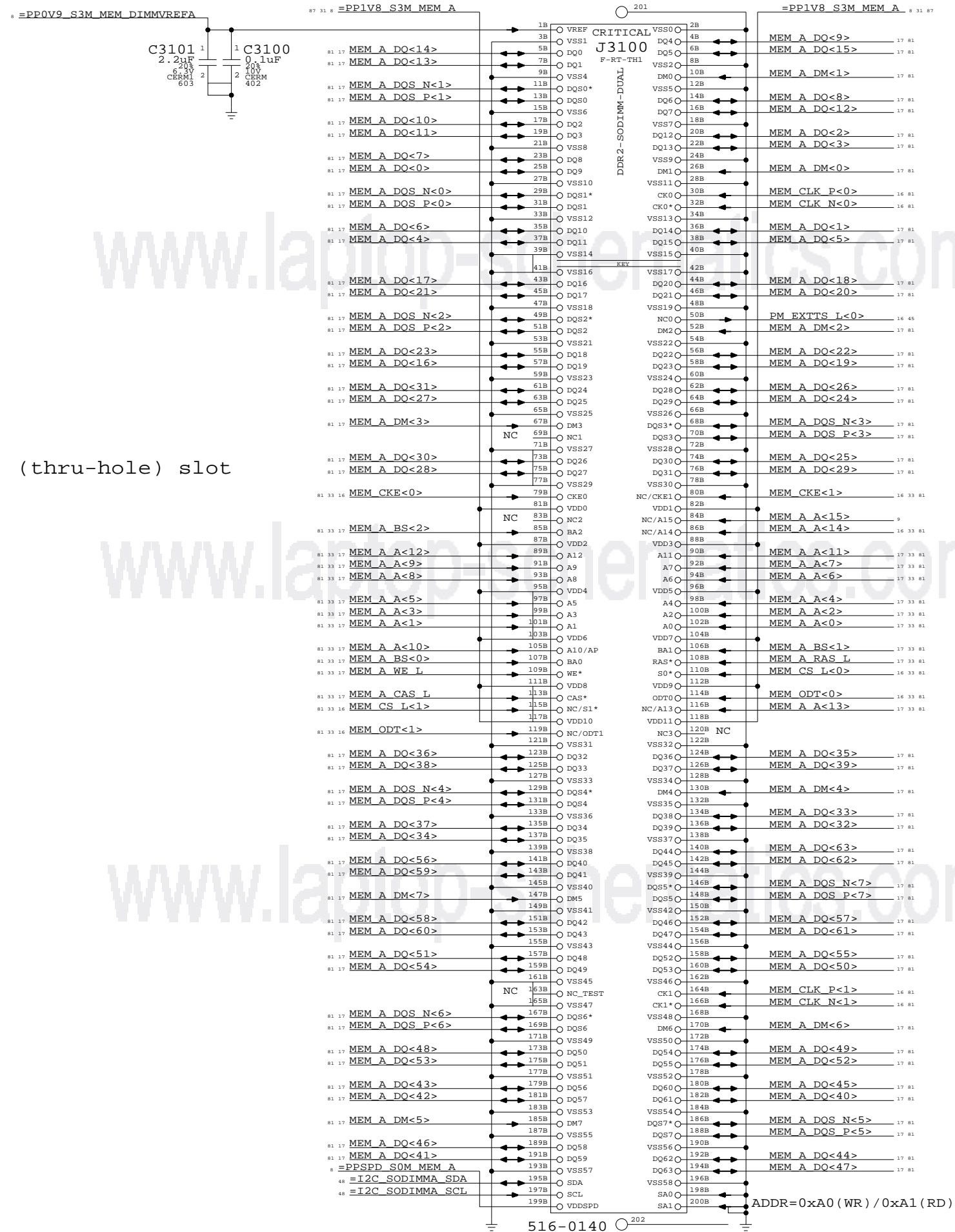
```
Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PPOV9_S3M_MEM_DIMMVFRA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)
```

---

```
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
```

---

```
BOM options provided by this page:
(NONE)
```



W7 31 8 =PP1V8 S3M MEM A

The diagram shows a 4x4 grid of capacitors on a PCB. The top-left corner is connected to a net labeled "PP1V8 S3M MEM A". The capacitors are arranged in four rows and four columns:

- Row 1:** C3108 (100UF, 20%, 6.3V, CERM 603), C3109 (100UF, 20%, 6.3V, CERM 603), C3110 (1UF, 10%, 6.3V, CERM 402), C3111 (1UF, 10%, 6.3V, CERM 402).
- Row 2:** C3112 (1UF, 10%, 6.3V, CERM 402), C3113 (1UF, 10%, 6.3V, CERM 402), C3114 (1UF, 10%, 6.3V, CERM 402), C3115 (1UF, 10%, 6.3V, CERM 402).
- Row 3:** C3116 (1UF, 10%, 6.3V, CERM 402), C3117 (1UF, 10%, 6.3V, CERM 402), C3118 (1UF, 10%, 6.3V, CERM 402), C3119 (1UF, 10%, 6.3V, CERM 402).
- Row 4:** C3120 (1UF, 10%, 6.3V, CERM 402), C3121 (1UF, 10%, 6.3V, CERM 402).

The capacitors are connected to a common ground plane at the bottom of the grid.

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## Page Notes

Power aliases required by this page:

- =PP1V8\_S3M\_MEM\_B  
- =PP0V9\_S3M\_MEM\_DIMMVREFB  
- =PPSPD\_S0M\_MEM\_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMB\_SCL  
- =I2C\_SODIMMB\_SDA

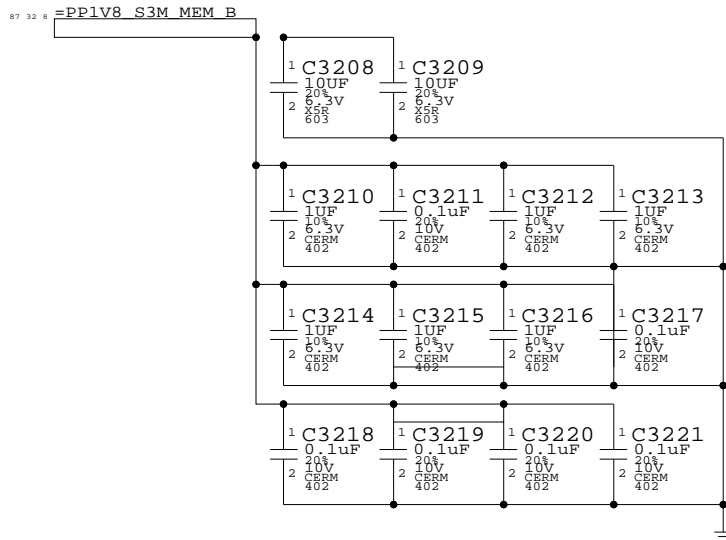
BOM options provided by this page:

(NONE)

"Expansion" (surface-mount) slot

## DDR2 Bypass Caps

(For return current)



## DDR2 SO-DIMM Connector B

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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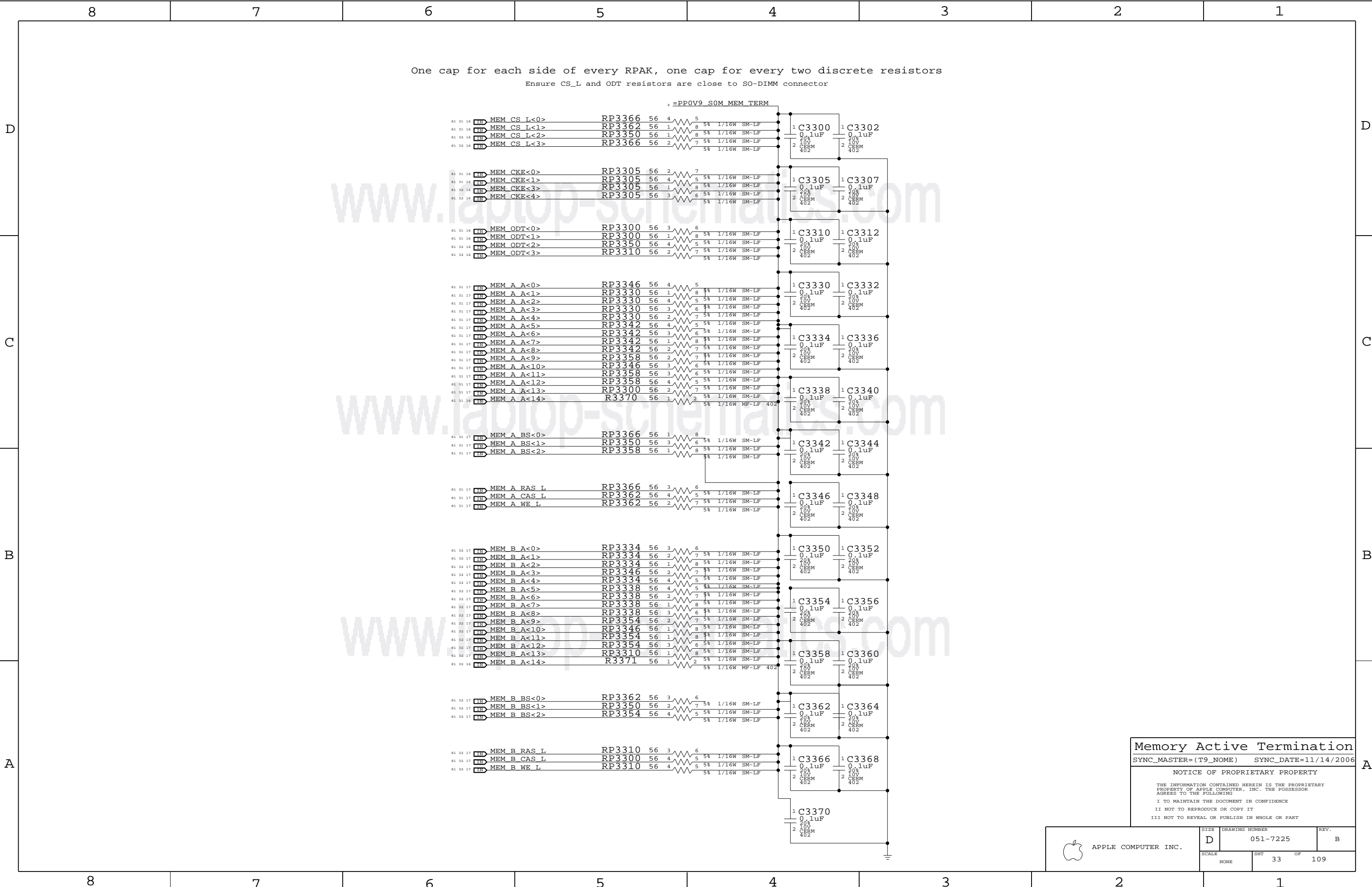


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Memory Active Termination

SYNC\_MASTER=(T9\_NOME) SYNC\_DATE=11/14/2006

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SCALE NONE SHT 33 OF 109

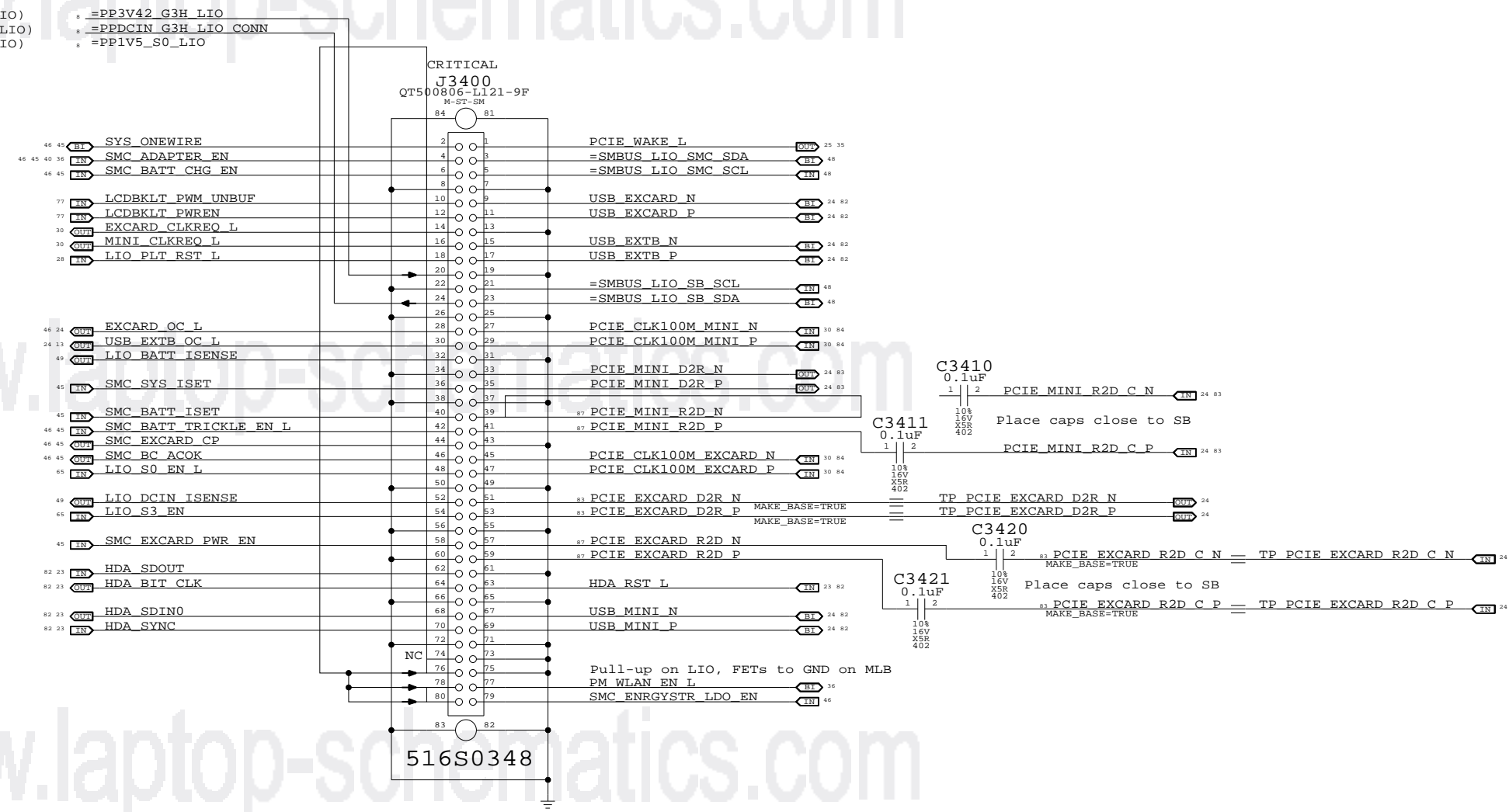


Left I/O Board Connector

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Left I/O Board Connector

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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NONE	34	109

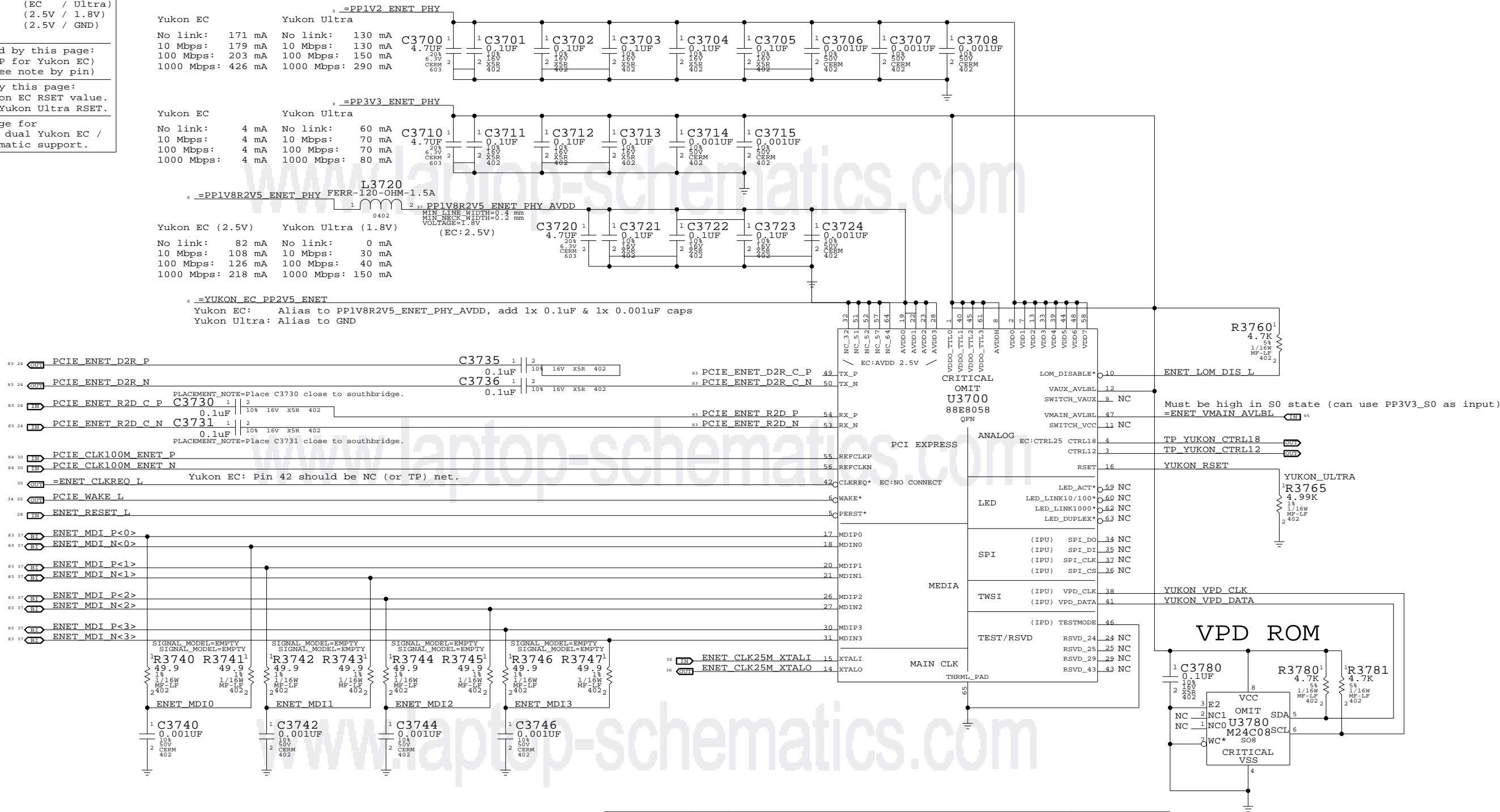
## Page Notes

Power aliases required by this page:  
- =PP3V3\_ENET\_PHY (EC / Ultra)  
- =PP1V8R2V5\_ENET\_PHY (2.5V / 1.8V)  
- =YUKON\_EC\_PP2V5\_ENET (2.5V / GND)  
- =PP1V2\_ENET\_PHY

Signal aliases required by this page:  
- =ENET\_CLKREQ\_L (NC/TP for Yukon EC)  
- =ENET\_VMAIN\_AVLBL (See note by pin)

BOM options provided by this page:  
YUKON\_EC - Selects Yukon EC RSET value.  
YUKON\_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON\_EC\_PP2V5\_ENET to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5\_ENET\_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET\_CLKREQ\_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON\_ULTRA)
- Use YUKON\_EC and YUKON\_ULTRA BOMOPTIONS to select stuffed part

### Ethernet (Yukon)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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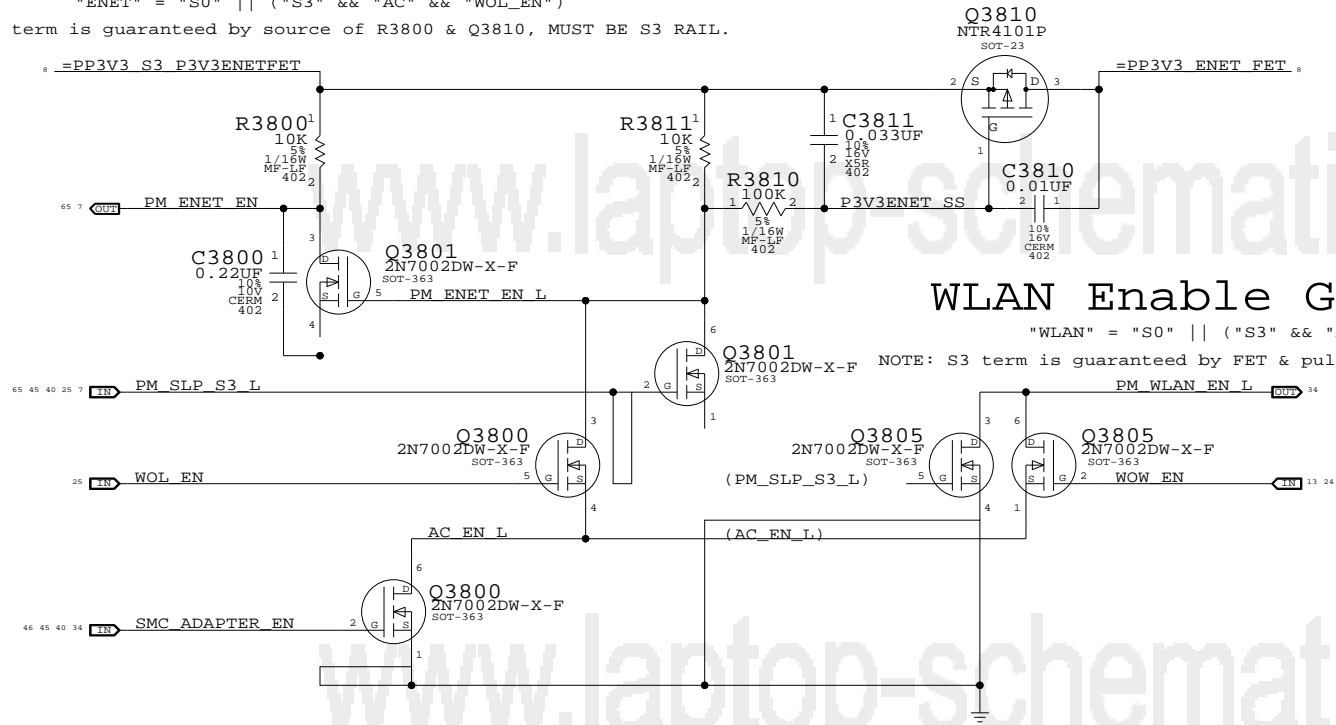
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. B

SCALE NONE SHT 37 OF 109

## ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL\_EN")  
NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



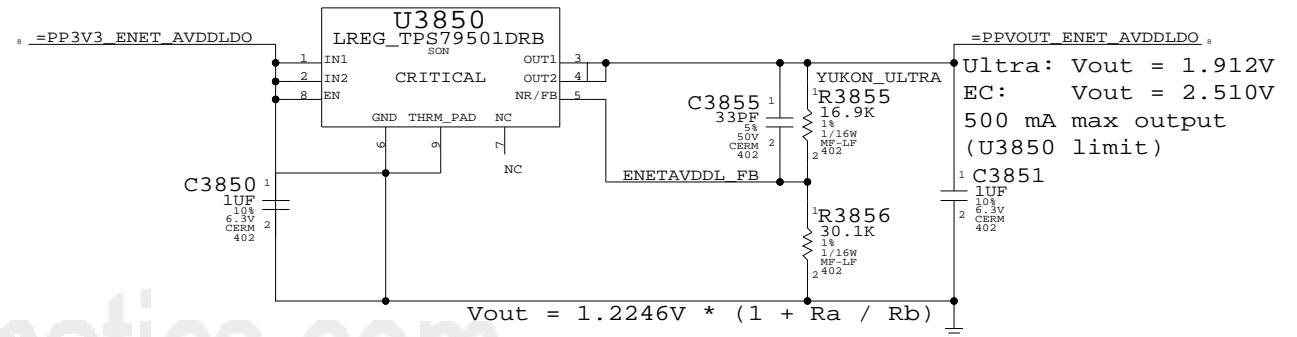
## 3.3V ENET FET

## WLAN Enable Generation

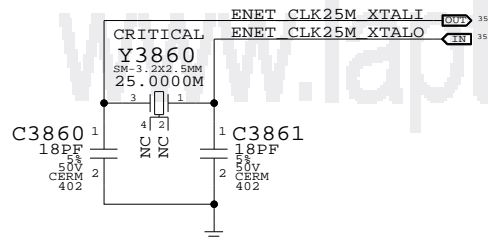
"WLAN" = "S0" || ("S3" && "AC" && "WOW\_EN")  
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

## Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC  
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



## Yukon Crystal



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

## Yukon Power Control

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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SIZE D DRAWING NUMBER 051-7225 REV. B

SCALE NONE SHT 38 OF 109

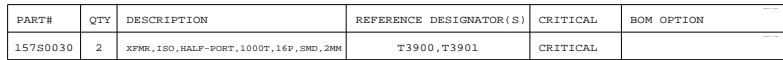
Power aliases required by this page:  
=GND\_CHASSIS\_ENET

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Signal aliases required by this page:  
(NONE)

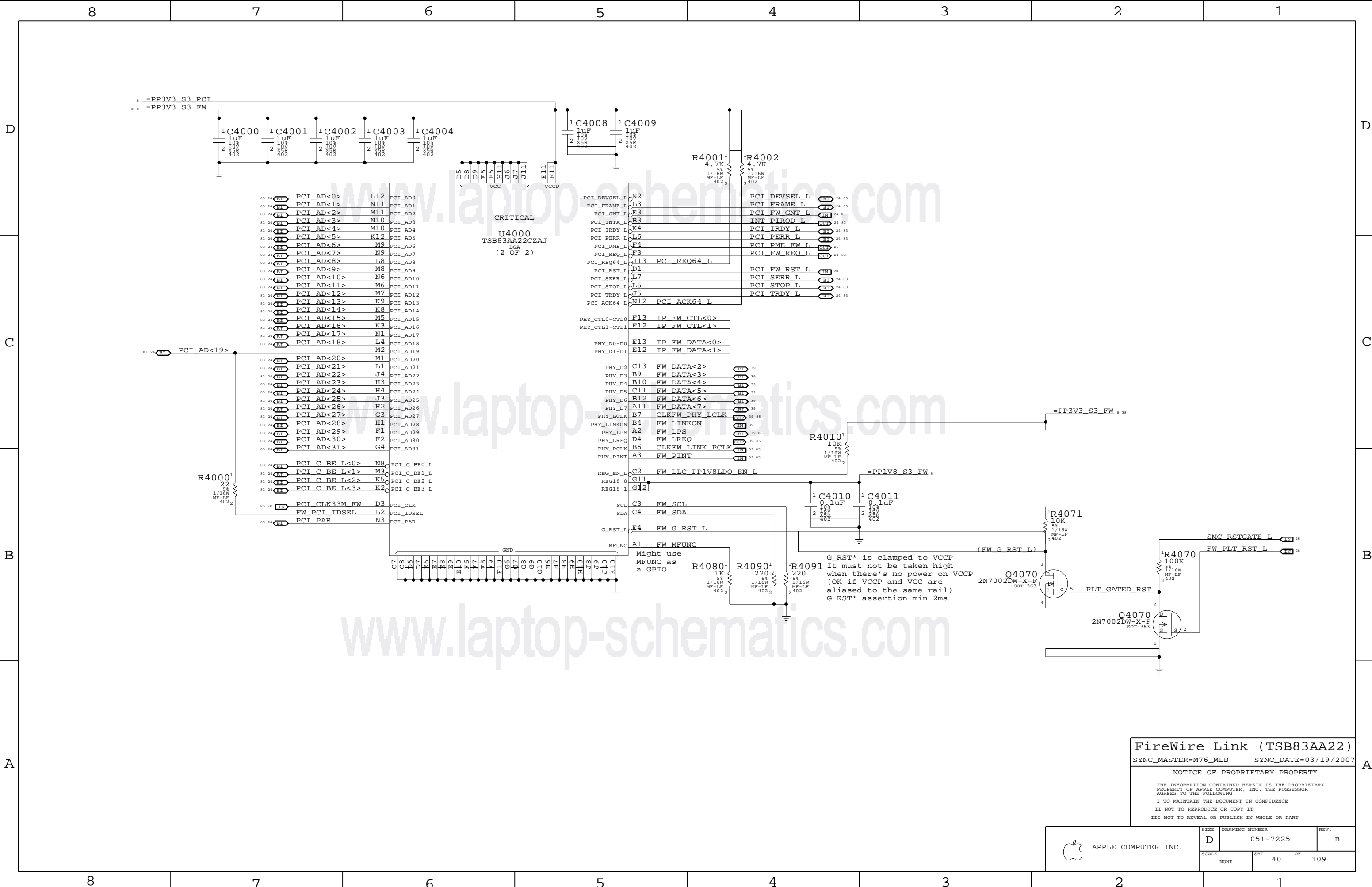
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BOM options provided by this page:  
(NONE)



<b>Ethernet Connector</b>	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. B
	SCALE NONE	SHT 39 OF 109	



FireWire Link (TSB83AA22)

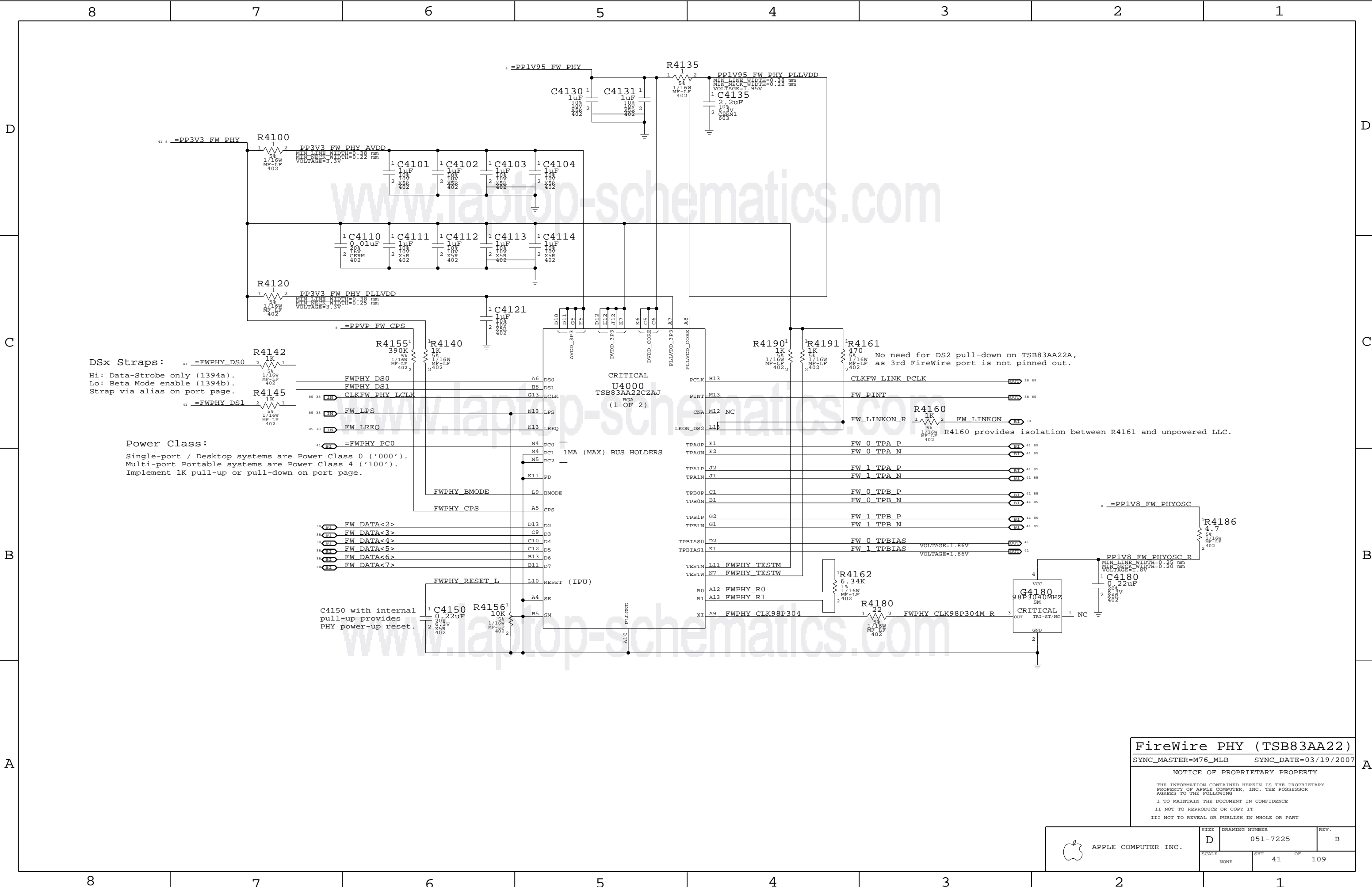
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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	D	051-7225	B
SCALE		SHT	OF
NONE		40	109





DSx Straps:

Hi: Data-Strobe only (1394a).  
Lo: Beta Mode enable (1394b).  
Strap via alias on port page.

Power Class:

Single-port / Desktop systems are Power Class 0 ('000').  
Multi-port Portable systems are Power Class 4 ('100').  
Implement 1K pull-up or pull-down on port page.

FireWire PHY (TSB83AA22)

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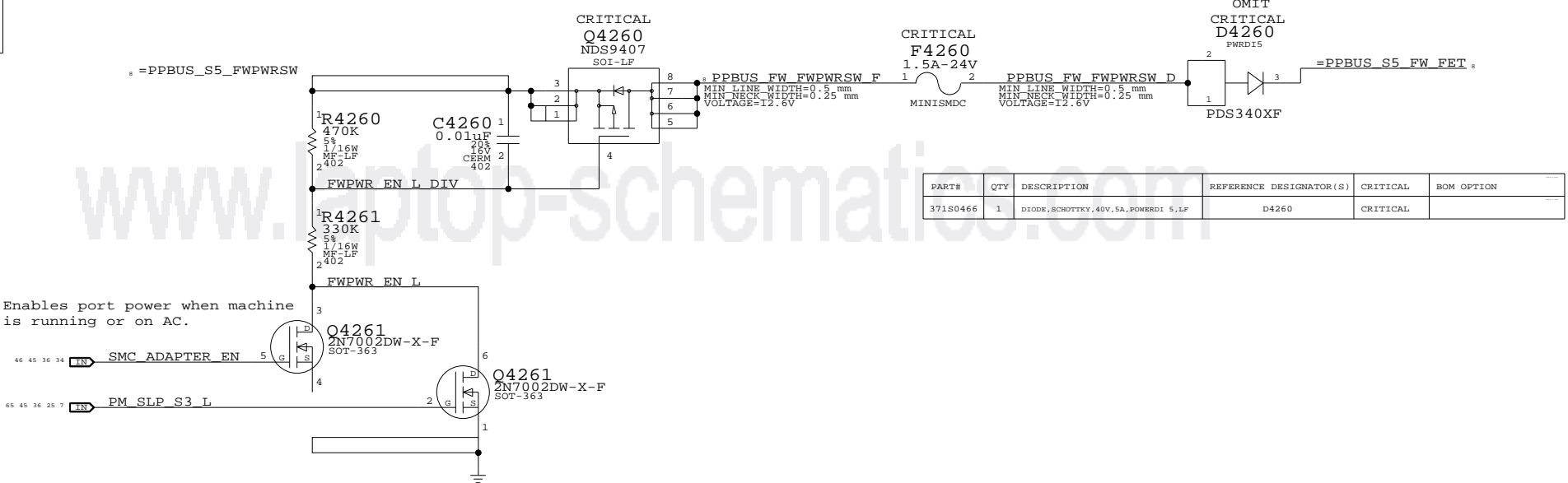
SIZE D DRAWING NUMBER 051-7225 REV. B

SCALE NONE SHT 41 OF 109

Page Notes

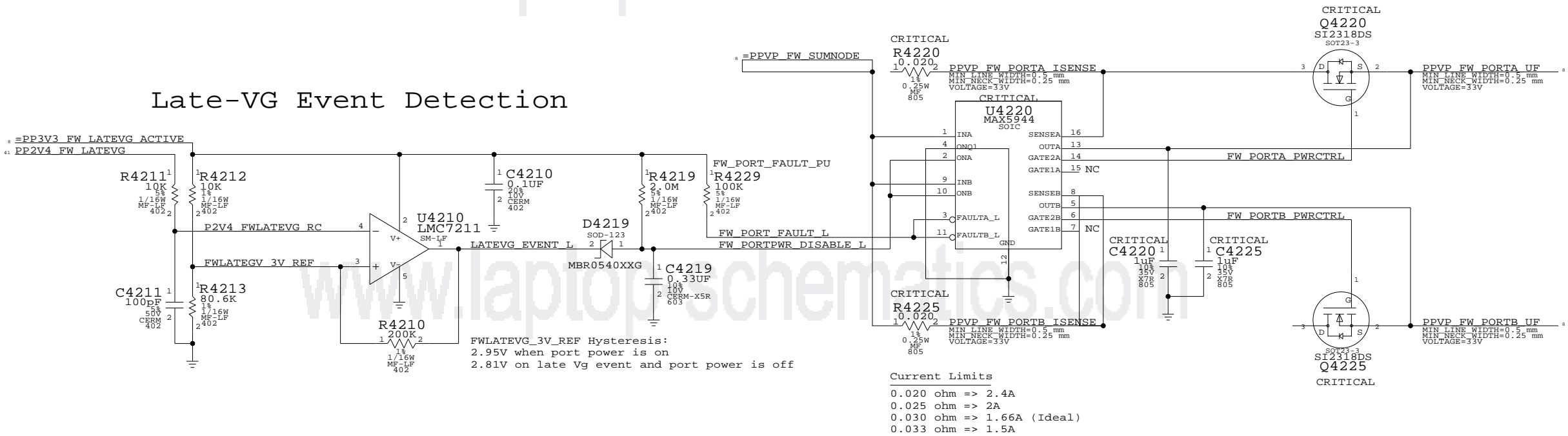
Power aliases required by this page:  
- =PPBUS\_S5\_FWPWSW (system supply for bus power)  
- =PP3V3\_FW\_LATEVG\_ACTIVE  
- =PPVP\_FW\_SUMNODE (power passthru summation node)  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
- FW\_PORT\_FAULT\_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



FireWire Port Power

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	B
SCALE	SHT	OF
NONE	42	109



2 1 1 P5VODD SS

58 1.16W 5% 402

10K 1% 402

(ODD has internal 100K pull-up to 5V)

42 ODD\_RST\_BUF L

CRITICAL J4400 M-ST-SM1-LF

1 50

2 49

3 48

IDE PDD<7>

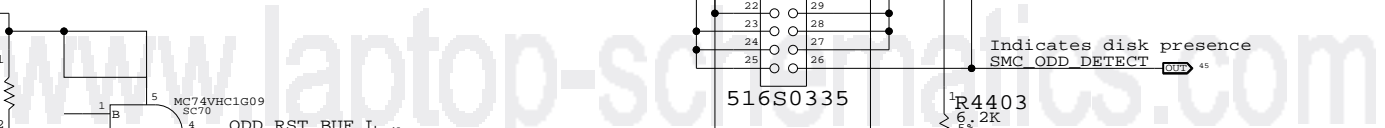
IDE PDD<8>

IDE PDD<9>

23 82

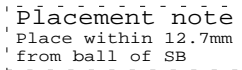
23 82

23 82



Unused SATA Ports

02 23	14	SATA B R2D C P	=	TP SATA B R2DP
				MAKE_BASE=TRUE
02 23	15	SATA B R2D C N	=	TP SATA B R2DN
				MAKE_BASE=TRUE



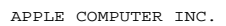
<sup>1</sup>R4460  
24.9  
18  
1/16W  
MF-LF  
2402

SYNC\_MASTER= ( MASTER )            SYNC\_DATE= ( MASTER )

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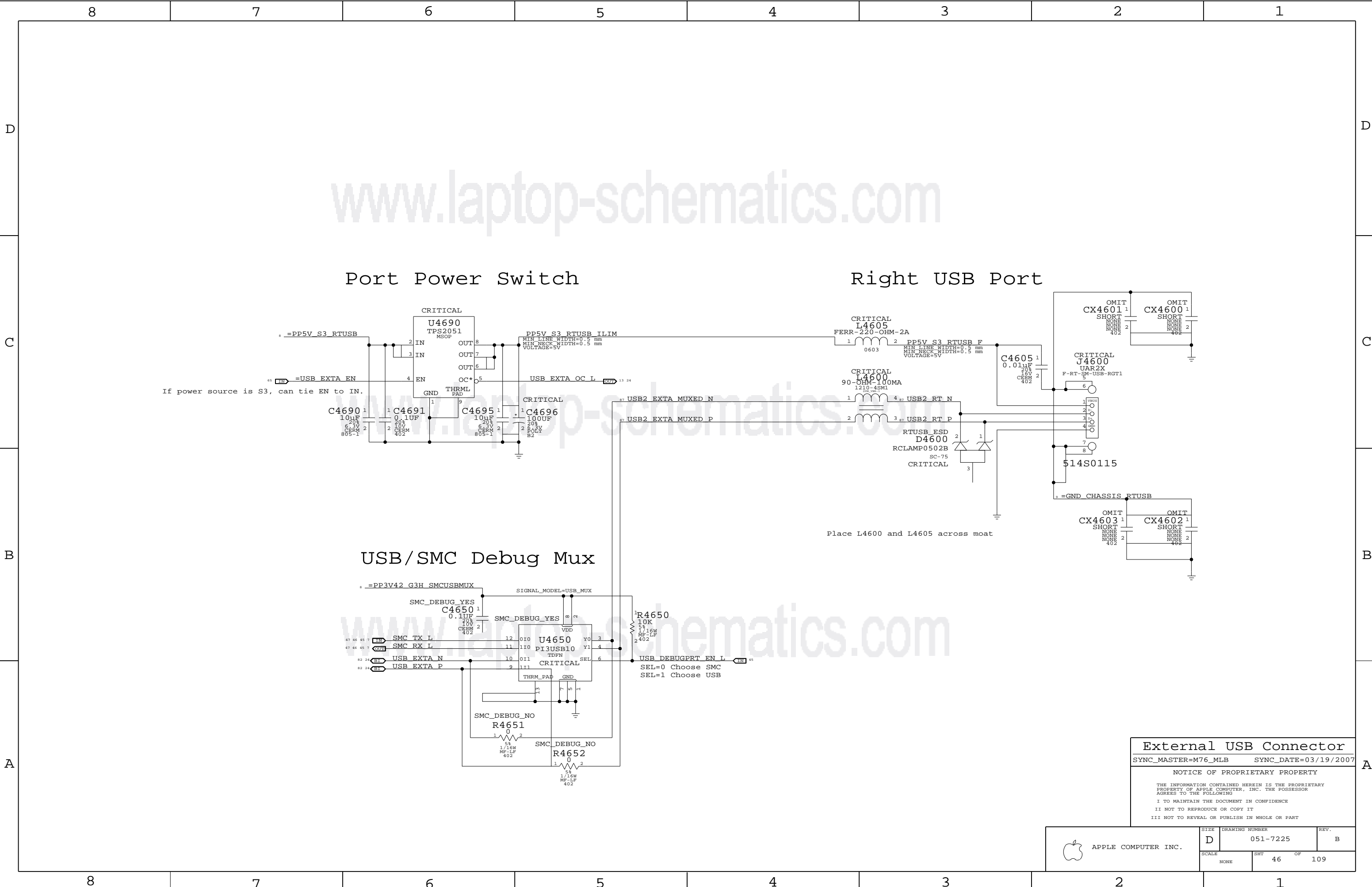


D	051-7225	B
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SCALE	SHT	OF
	44	109

NONE	11	109
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Port Power Switch

Right USB Port

USB/SMC Debug Mux

External USB Connector

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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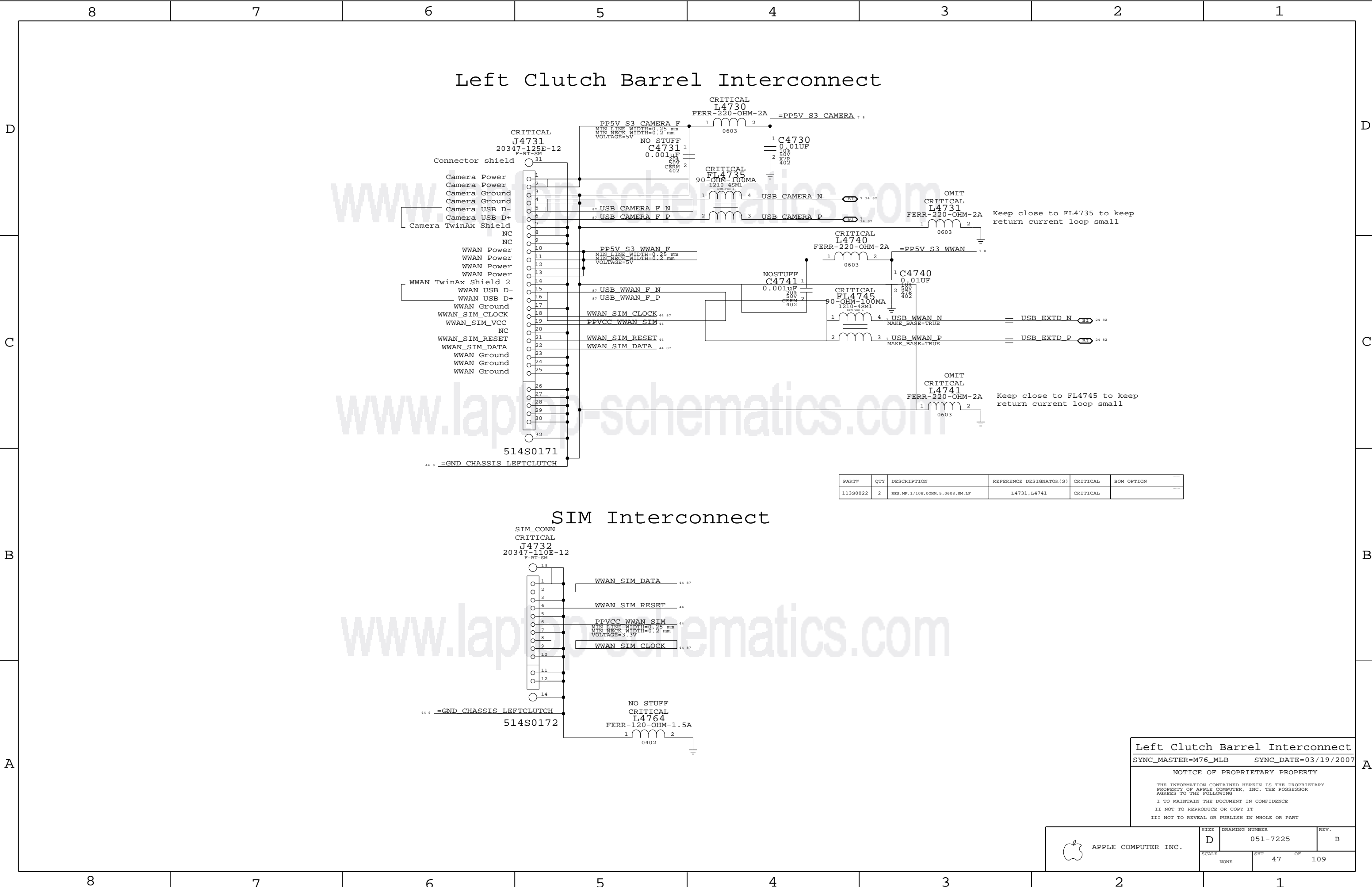
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SIZE D DRAWING NUMBER 051-7225 REV. B

SCALE NONE SHT 46 OF 109



Left Clutch Barrel Interconnect  
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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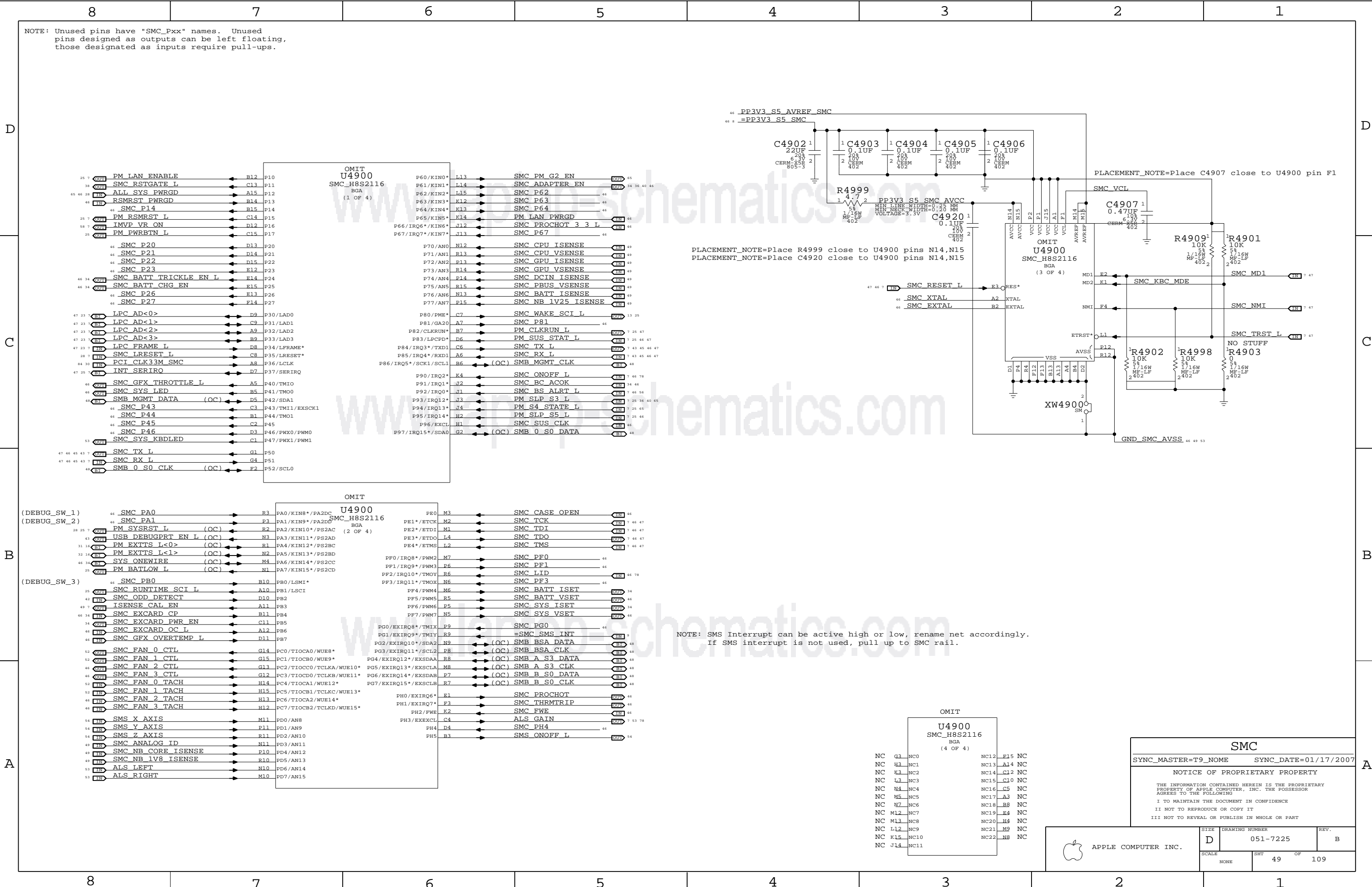
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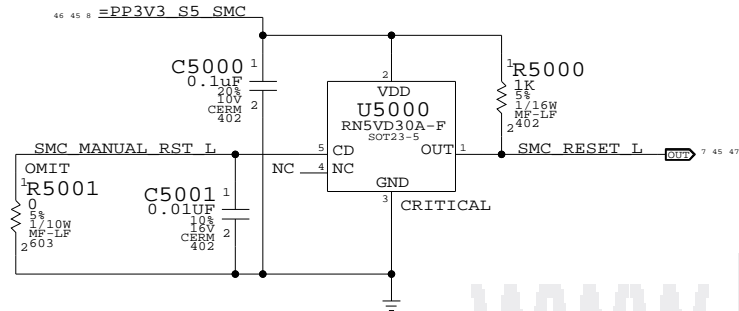
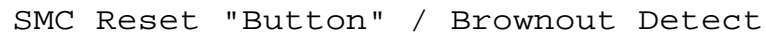
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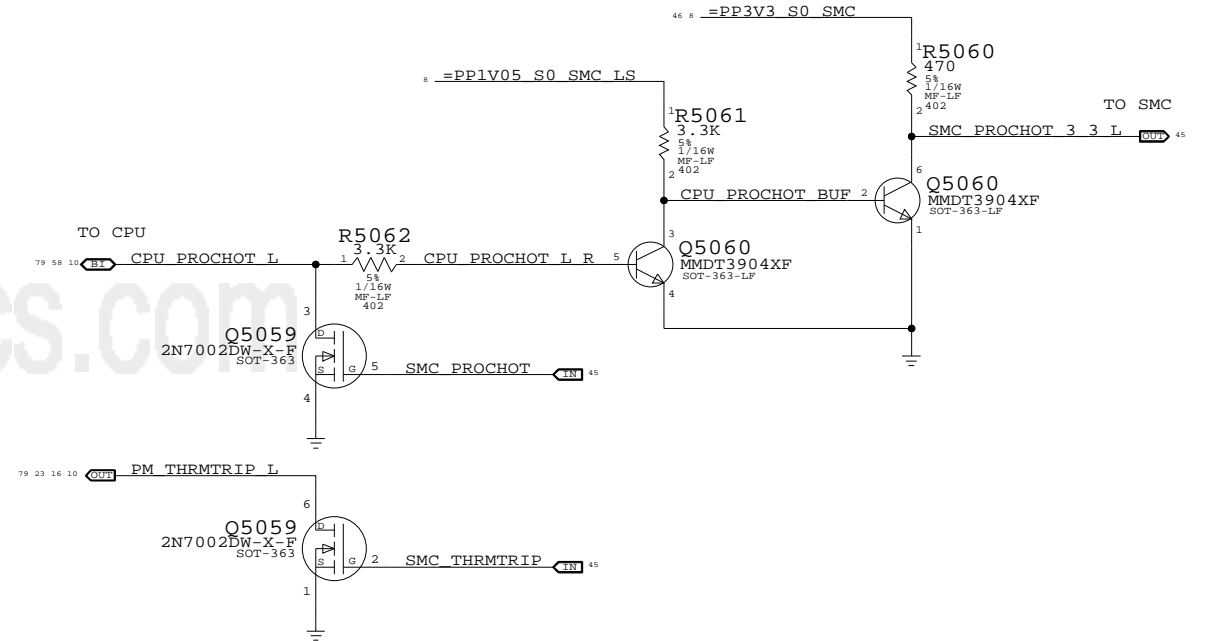
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. B
	SCALE NONE	SHT 47	OF 109



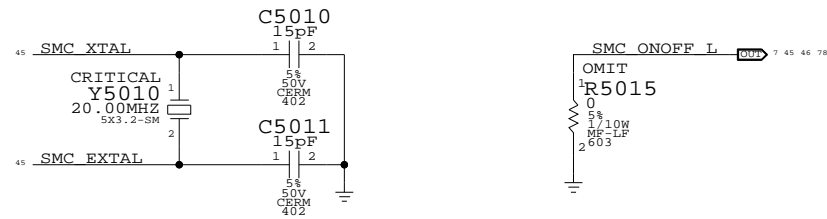
www.laptop-schematics.com



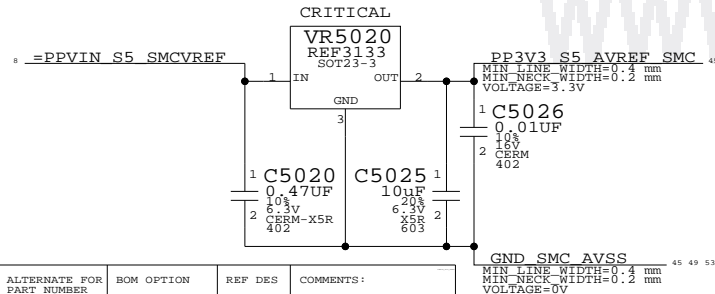
## SMC FSB to 3.3V Level Shifting



## SMC Crystal Circuit      Debug Power "Button"

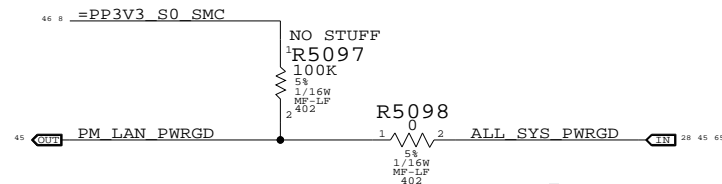


## SMC AVREF Supply



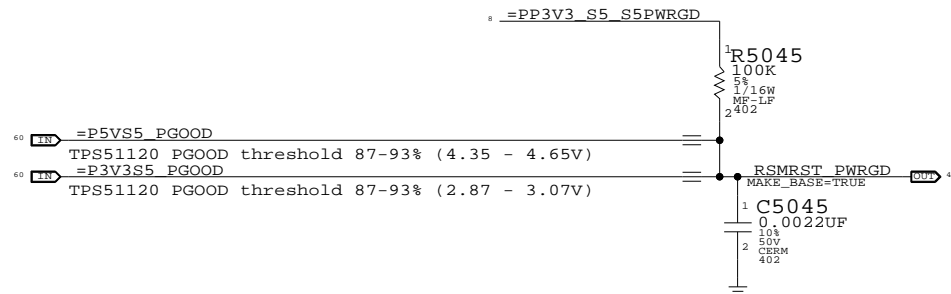
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

# LAN PWRGD Circuit

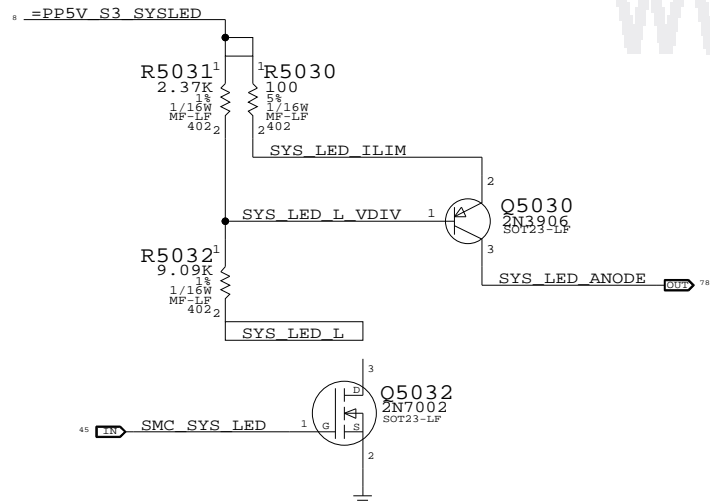


## S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



## System (Sleep) LED Circuit




46 45 8 =PP3V3 S5 SMC

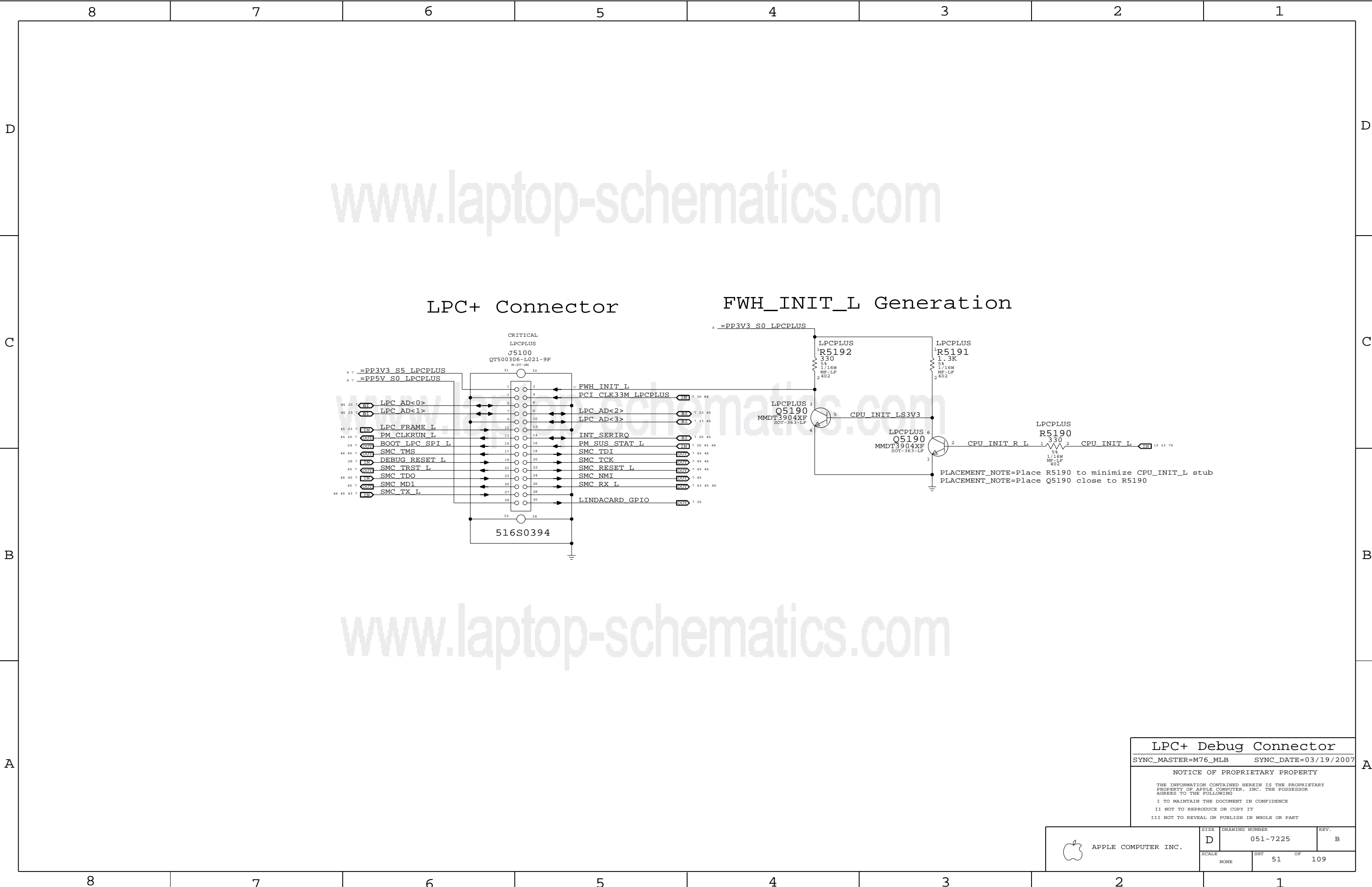
Component	Regulator	Resistor	Output	Capacitor
SMC PA0	R5091	100K	5V	1/16W MF-LF 402
SMC PA1	R5092	100K	5V	1/16W MF-LF 402
SMC PB0	R5093	100K	5V	1/16W MF-LF 402
SMC ONOFF L	R5070	10K	5V	1/16W MF-LF 402
SMC LID	R5071	100K	5V	1/16W MF-LF 402
SMC FWE	R5072	10K	5V	1/16W MF-LF 402
SMC TX L	R5073	10K	5V	1/16W MF-LF 402
SMC RX L	R5074	100K	5V	1/16W MF-LF 402
SYS ONEWIRE	R5075	2.0K	ONEWIRE PU	
SMC BS ALRT L	R5076	100K	5V	1/16W MF-LF 402
SMC TMS	R5077	10K	5V	1/16W MF-LF 402
SMC TDI	R5078	10K	5V	1/16W MF-LF 402
SMC TCK	R5079	10K	5V	1/16W MF-LF 402
SMC P67	R5081	10K	5V	1/16W MF-LF 402
SMC PF3	R5082	10K	5V	1/16W MF-LF 402
SMC PG0	R5083	10K	5V	1/16W MF-LF 402
SMC PH4	R5084	10K	5V	1/16W MF-LF 402
SMC BATT TRICKLE EN L	R5085	10K	5V	1/16W MF-LF 402
SMC BATT CHG EN	R5086	10K	5V	1/16W MF-LF 402
SMC ADAPTER EN	R5087	470K	5V	1/16W MF-LF 402
SMC CADAPE OPEN	R5088	10K	5V	1/16W MF-LF 402
SMC BC ACOK	R5089	100K	5V	1/16W MF-LF 402
SMC EXCARD CP	R5090	100K	5V	1/16W MF-LF 402
PM SUS STAT L				
PM SLP S5 L				

45	34	SMC BATT TRICKLE EN L	R5083	10K	1	1	2	5%	1/16W MF-LF 402	
45	34	SMC BATT CHG EN	R5084	10K	1	1	2	5%	1/16W MF-LF 402	
45	36	SMC ADAPTER EN	R5085	10K	1	1	2	5%	1/16W MF-LF 402	
45	36	SMC CASE OPEN	R5086	10K	1	1	2	5%	1/16W MF-LF 402	
45	34	SMC BC ACLK	R5087	470K	1	1	2	5%	1/16W MF-LF 402	
45	34	SMC EXCARD CP	R5088	10K	1	1	2	5%	1/16W MF-LF 402	
47	45	PM_S5_STAT L	R5089	100K	1	1	2	5%	1/16W MF-LF 402	
45	25	PM_SLP_S5 L	R5090	100K	1	1	2	5%	1/16W MF-LF 402	

<div>SMC Support</div>			
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	
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 <div>APPLE COMPUTER INC.</div>	SIZE	DRAWING NUMBER		REV.
	D	051-7225		B
	SCALE	SHT	OF	
NONE	50		109	





LPC+ Debug Connector

SYNC\_MASTER=M76\_MLB

SYNC\_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

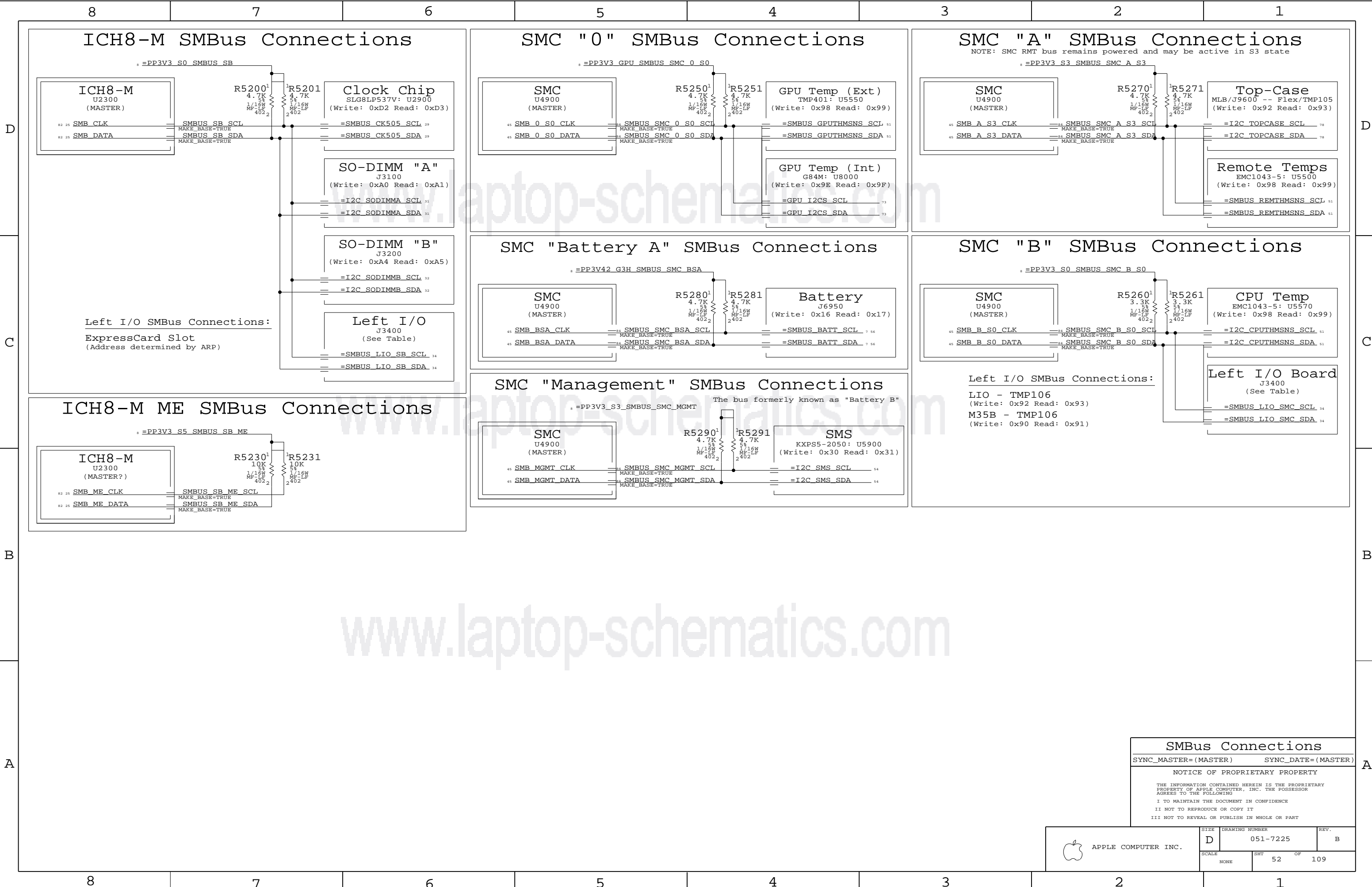
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	D	051-7225	B
SCALE		SHT	OF
NONE		51	109



SMBus Connections

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

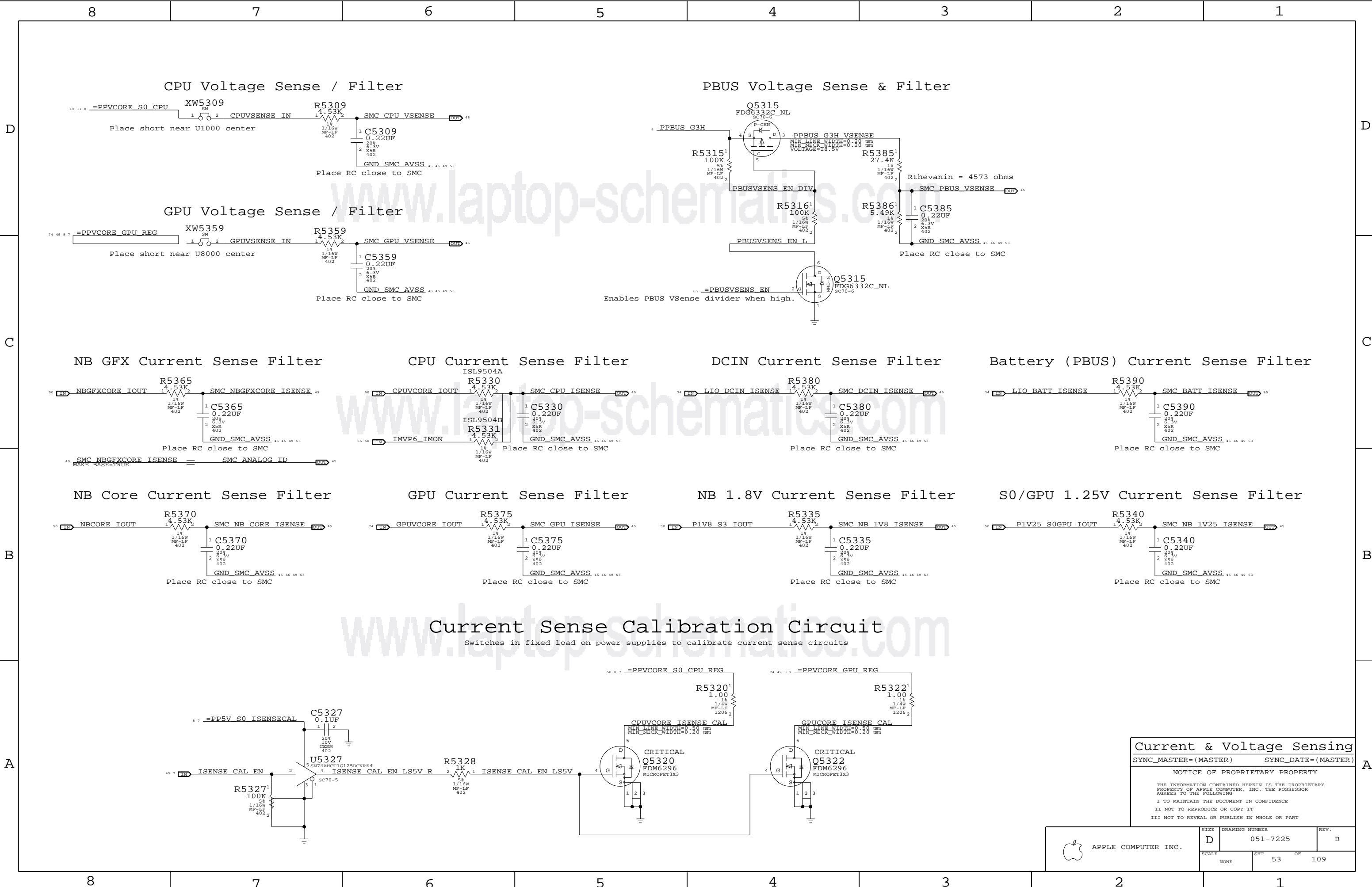
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	D	051-7225		B
SCALE		SHT	OF	
NONE		52	109	



Current & Voltage Sensing

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

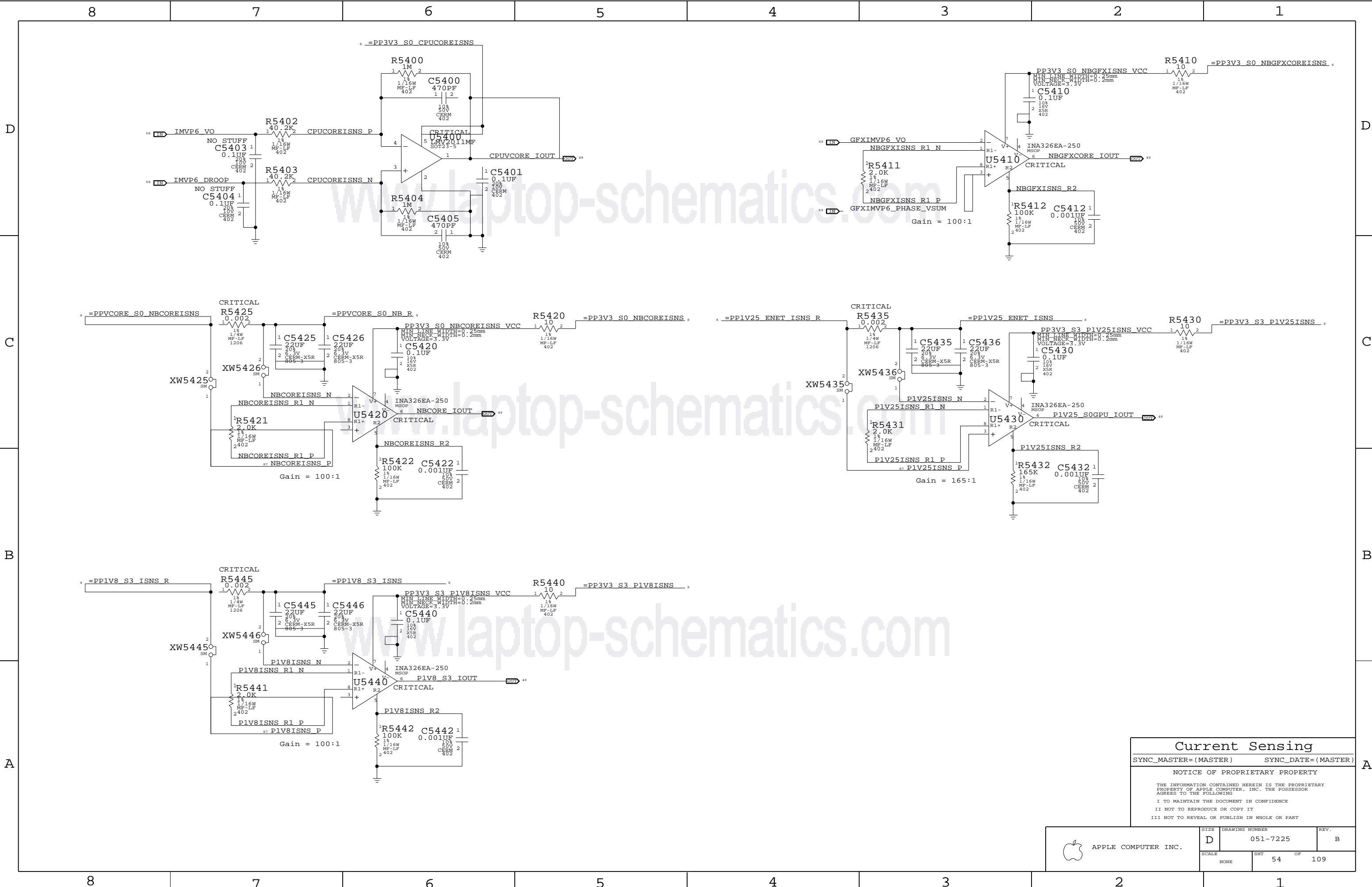
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SIZE	D	DRAWING NUMBER	051-7225	REV.	B
SCALE	NONE	SHT	53	OF	109



Current Sensing

SYNC\_MASTER= (MASTER)      SYNC\_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

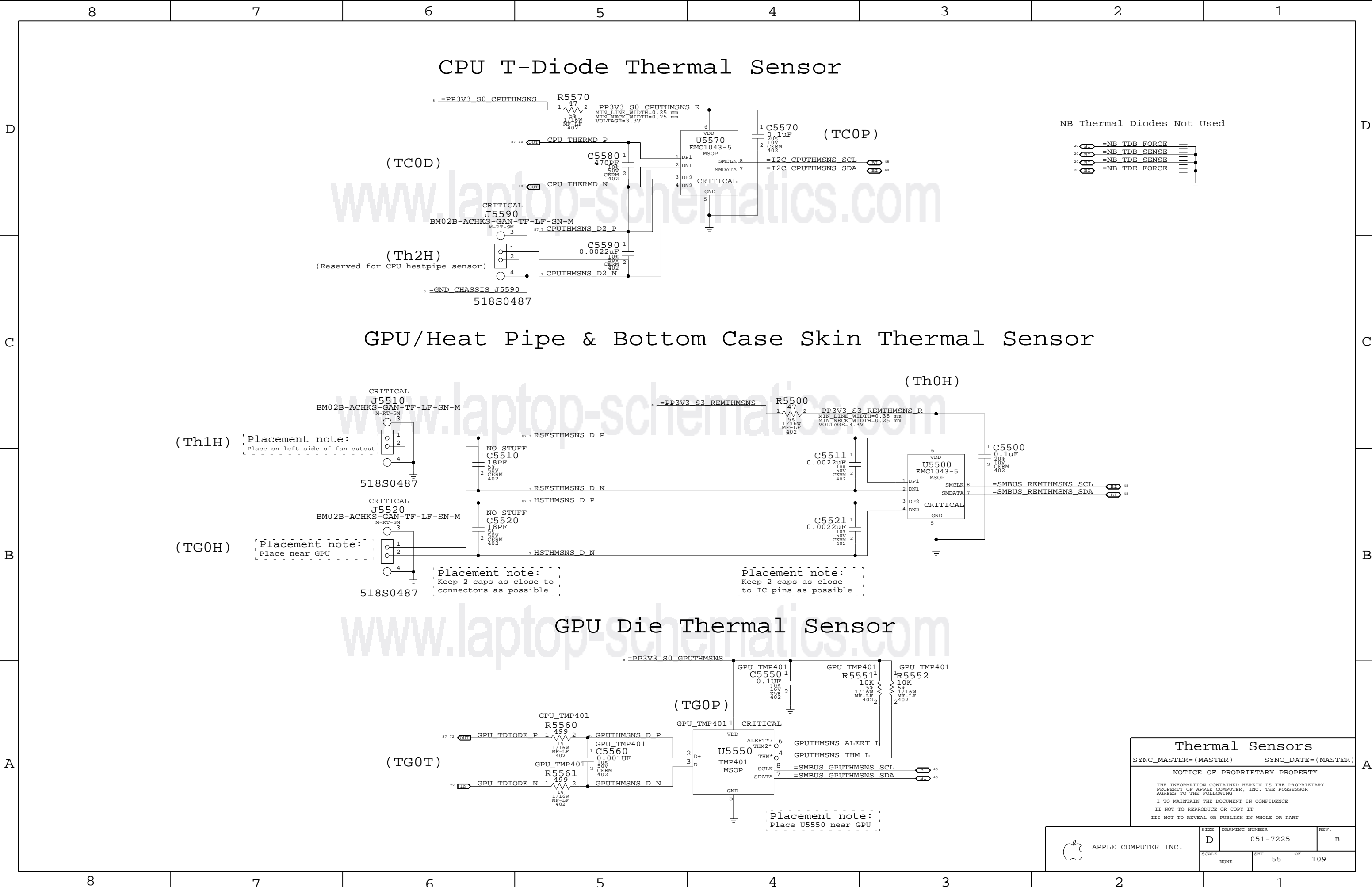
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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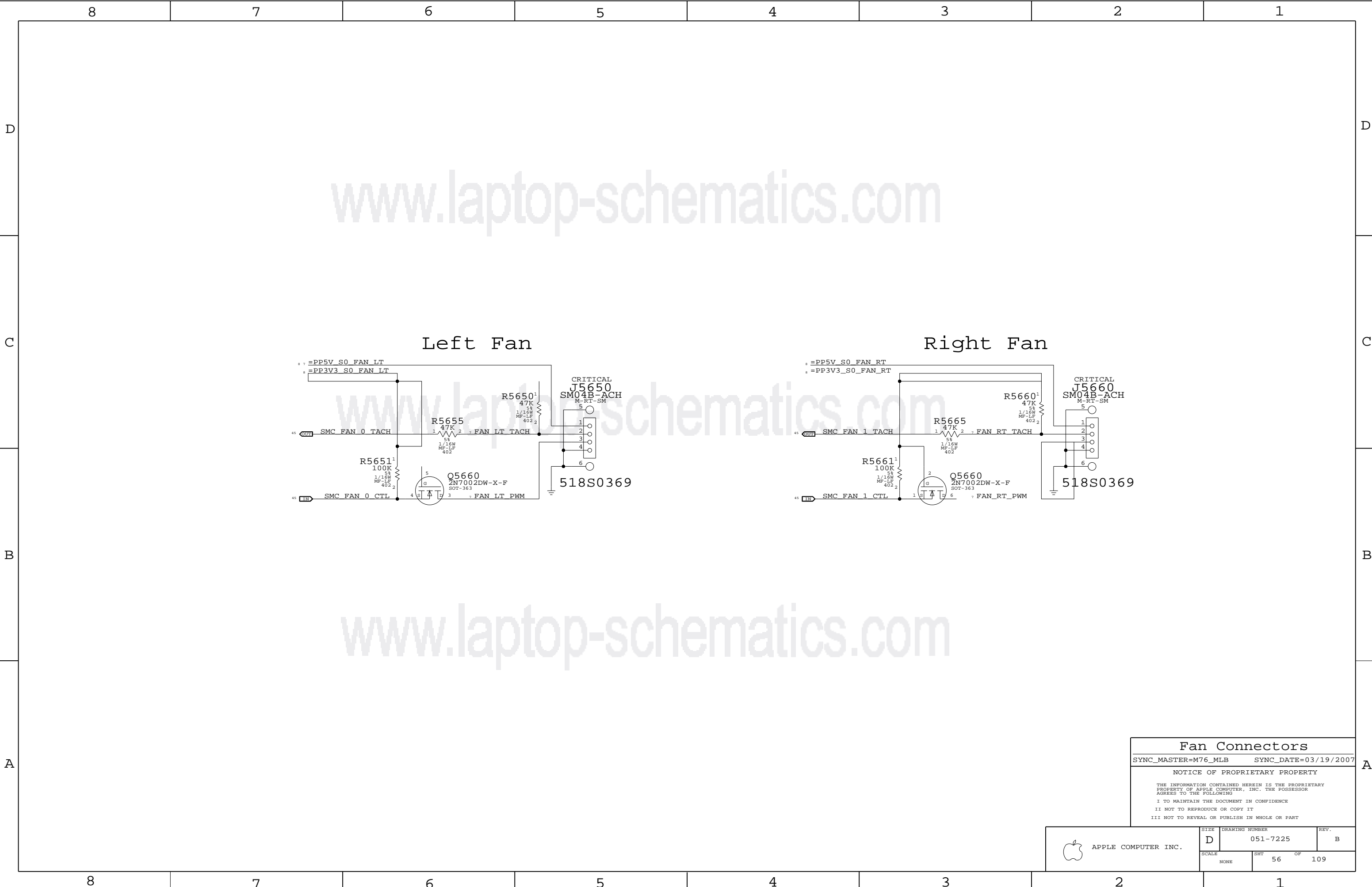
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	D	051-7225	B
SCALE		SHT	OF
NONE		54	109







Fan Connectors		
SYNC_MASTER=M76_MLB		SYNC_DATE=03/19/2007
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	SCALE NONE	SHT 56	OF 109

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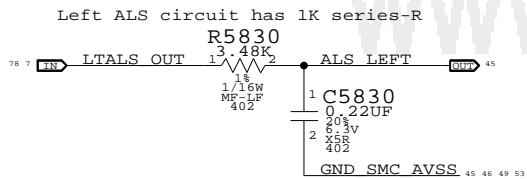
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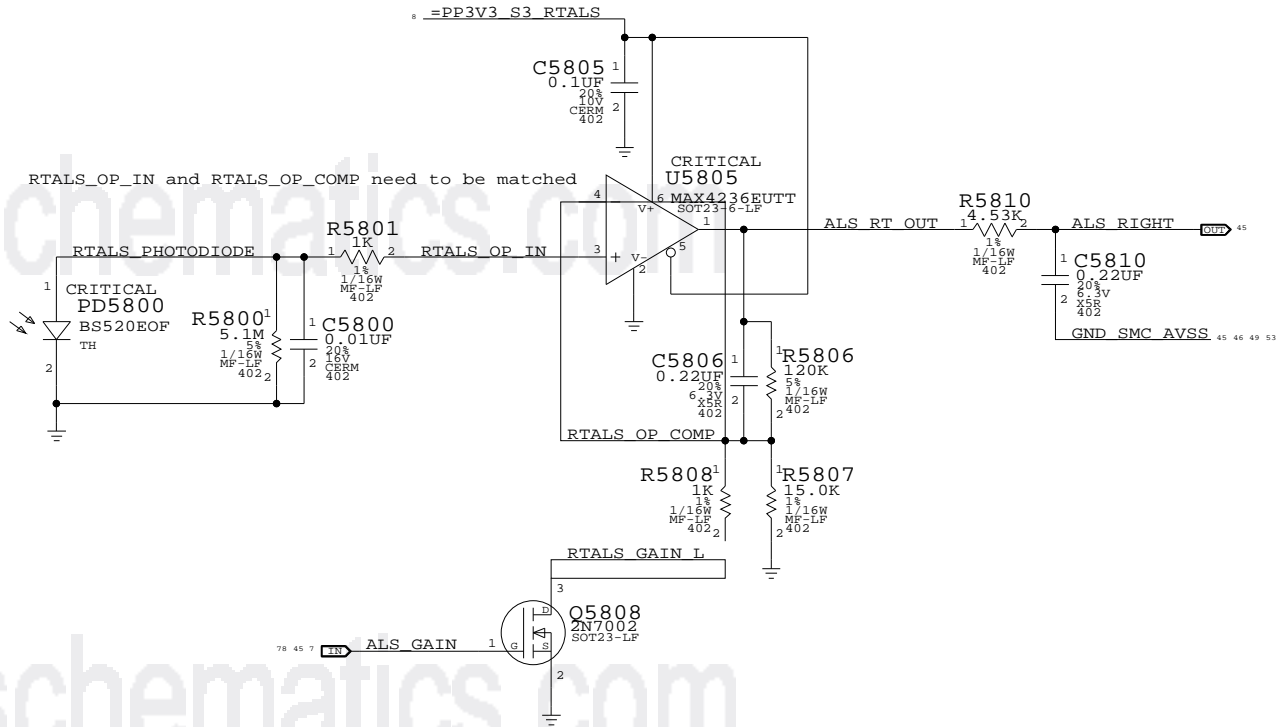
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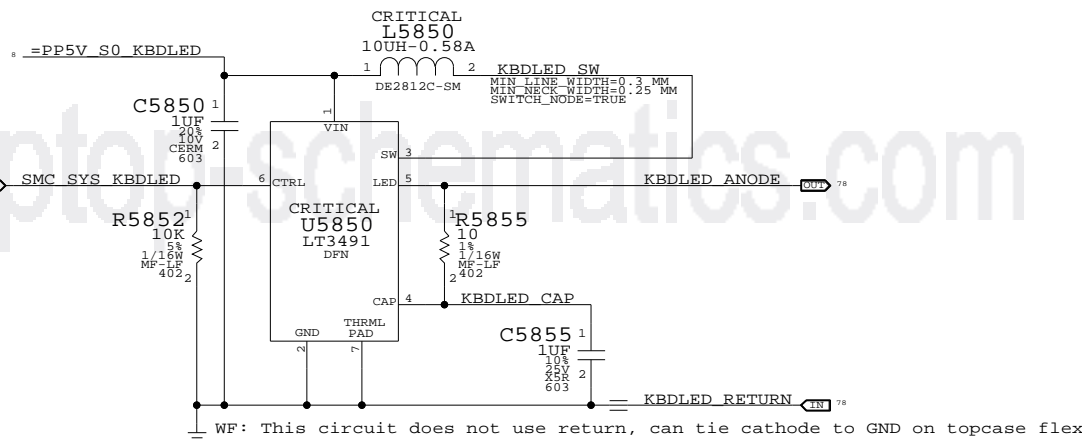
### Left ALS Filter



### Right ALS Circuit



### Keyboard LED Driver



#### ALS Support

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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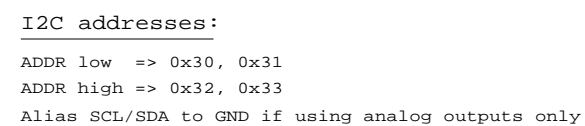


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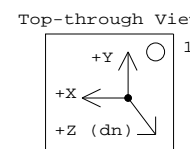
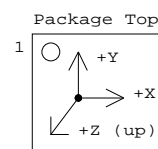
SIZE D DRAWING NUMBER 051-7225 REV. B

SCALE NONE SHT 58 OF 109


www.laptop-schematics.com

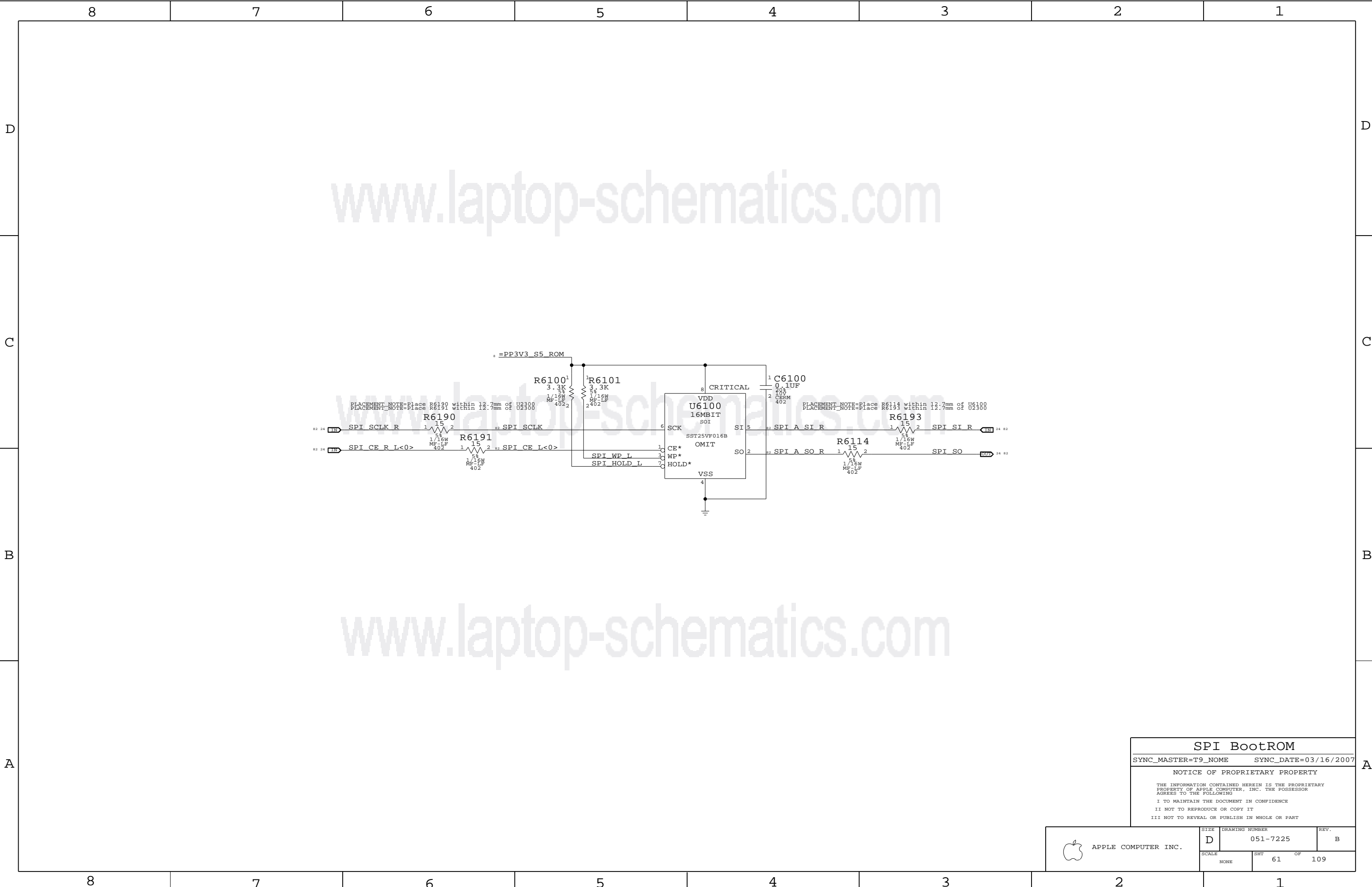


Desired orientation when  
placed on board bottom-side:



Sudden Motion Sensor (SMS)	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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SPI BootROM

SYNC\_MASTER=T9\_NOME

SYNC\_DATE=03/16/2007


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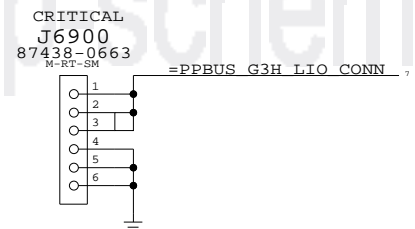
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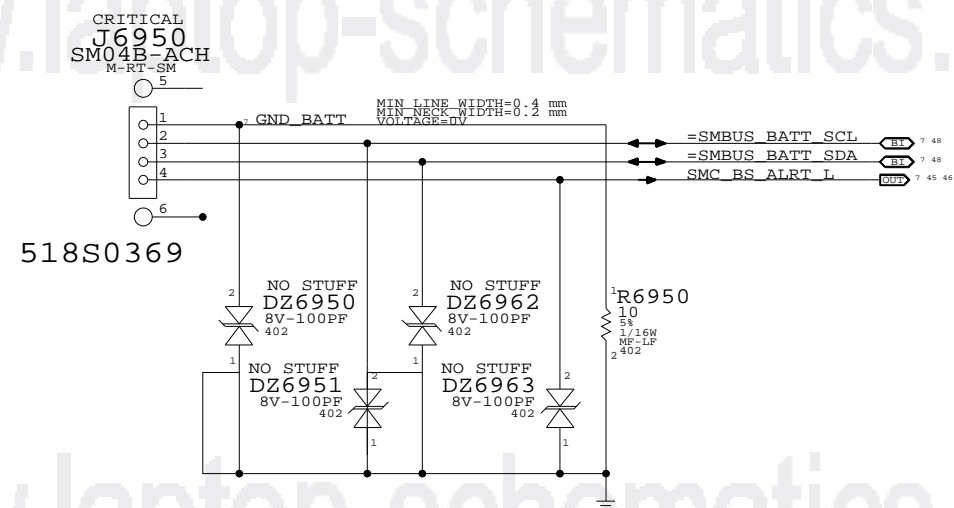
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. B
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518S0458

### Battery Connector (Digital Signals)



PBus-In & Battery Connectors

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=09/09/2006

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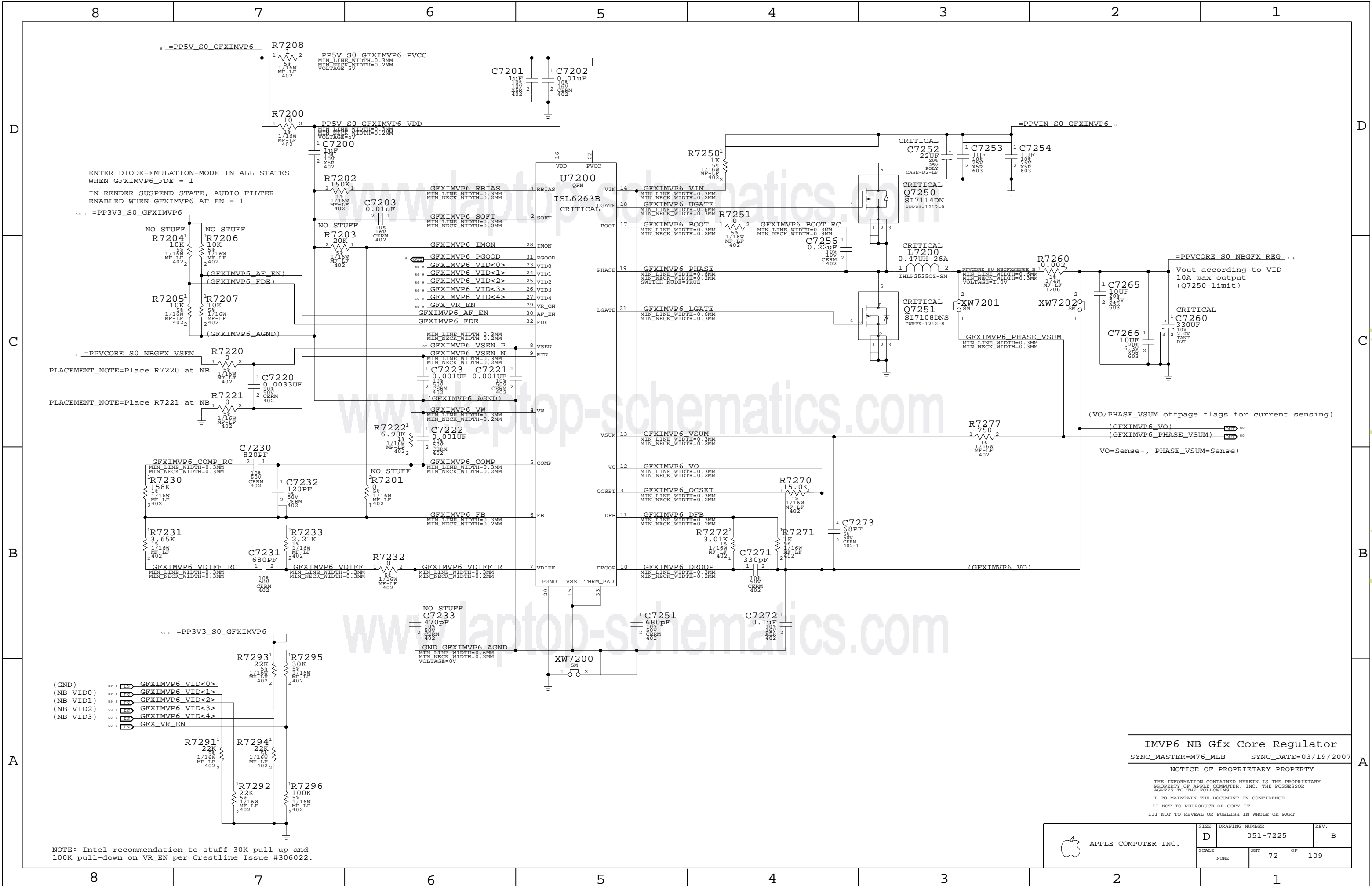


SIZE D	DRAWING NUMBER 051-7225	REV. B
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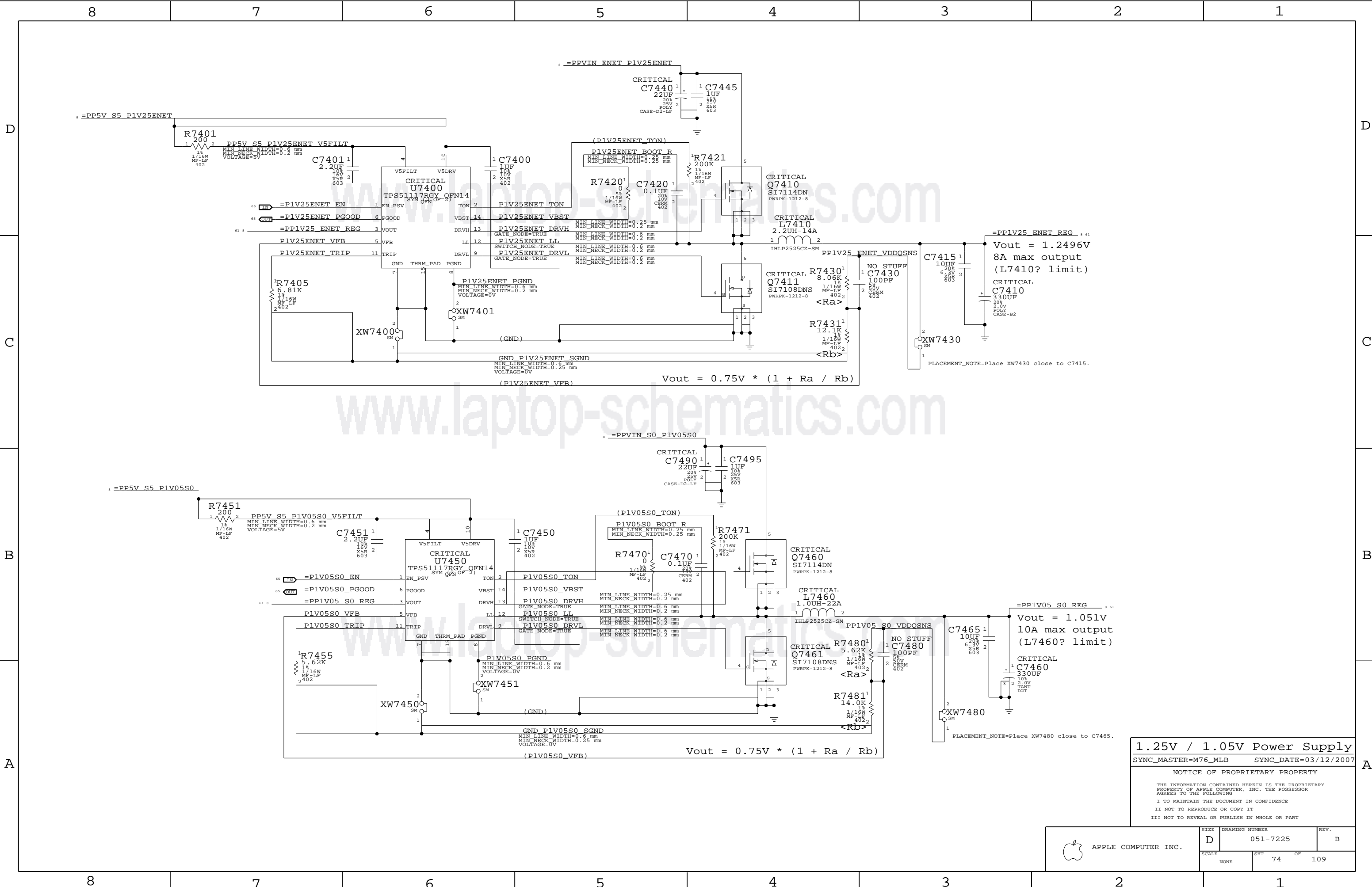












1.25V / 1.05V Power Supply

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007

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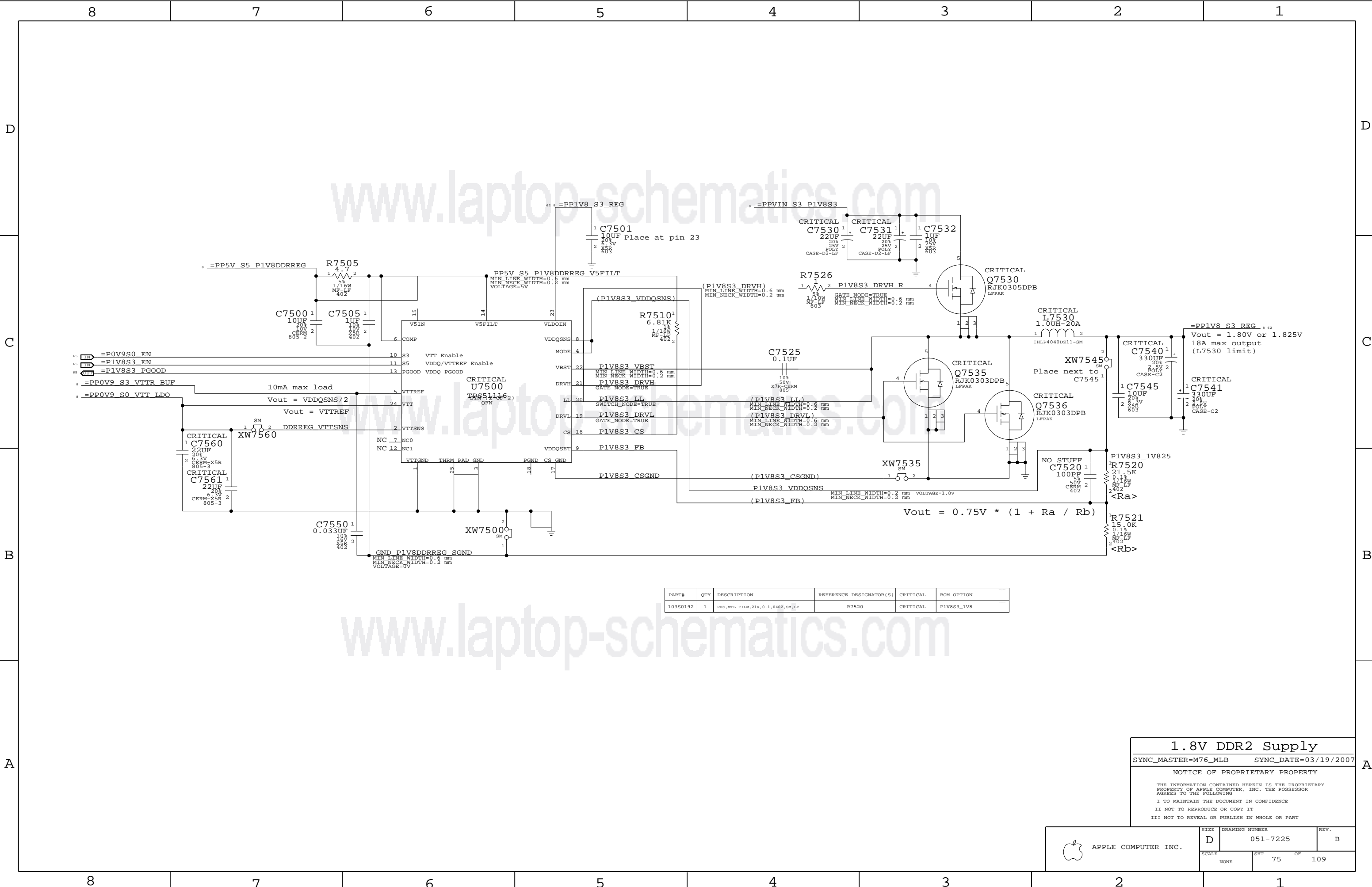
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SIZE	DRAWING NUMBER	REV.
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NONE	74	109





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	PIV8S3_1V8

1.8V DDR2 Supply

SYNC\_MASTER=M76\_MLB      SYNC\_DATE=03/19/2007

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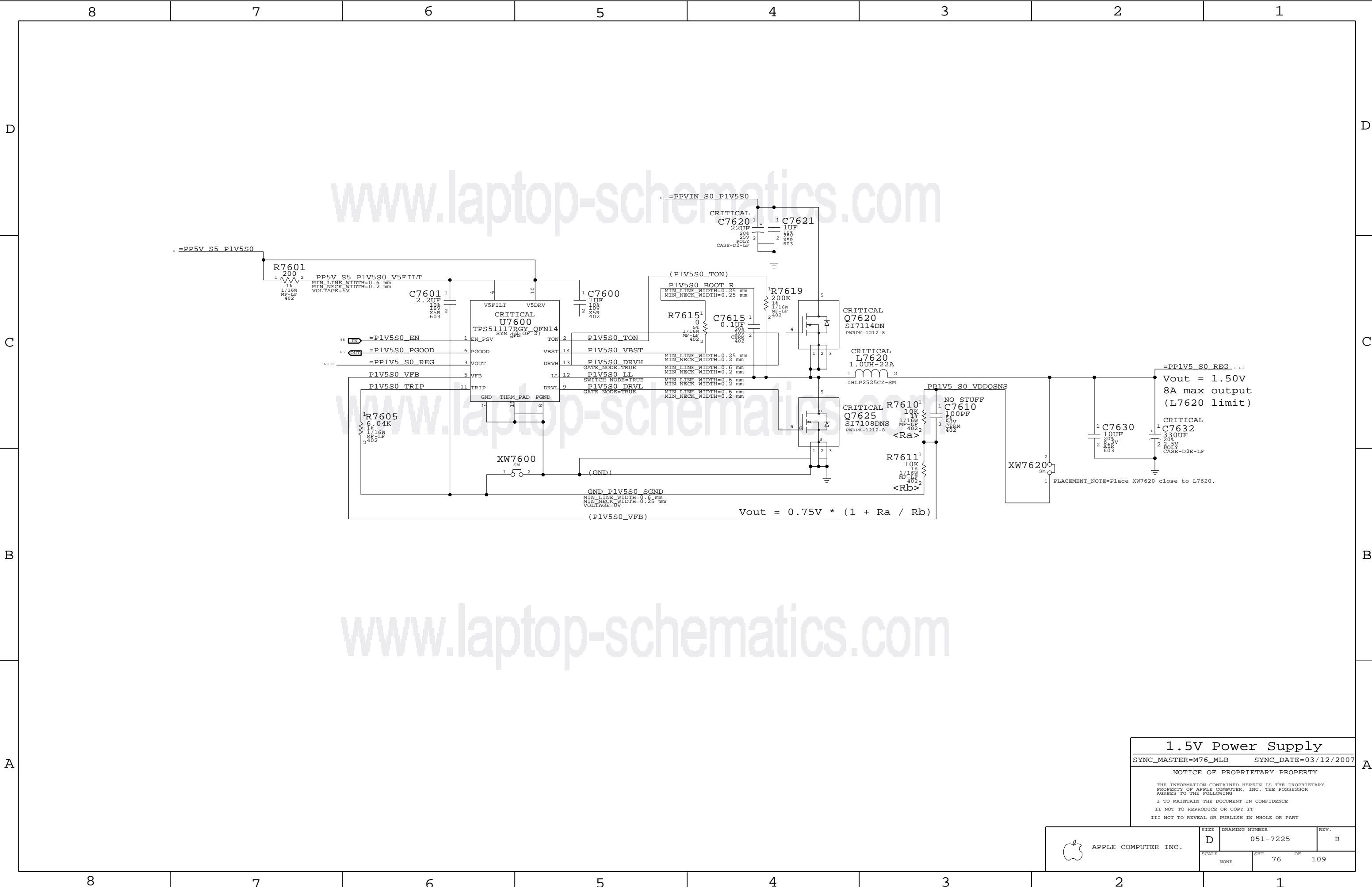
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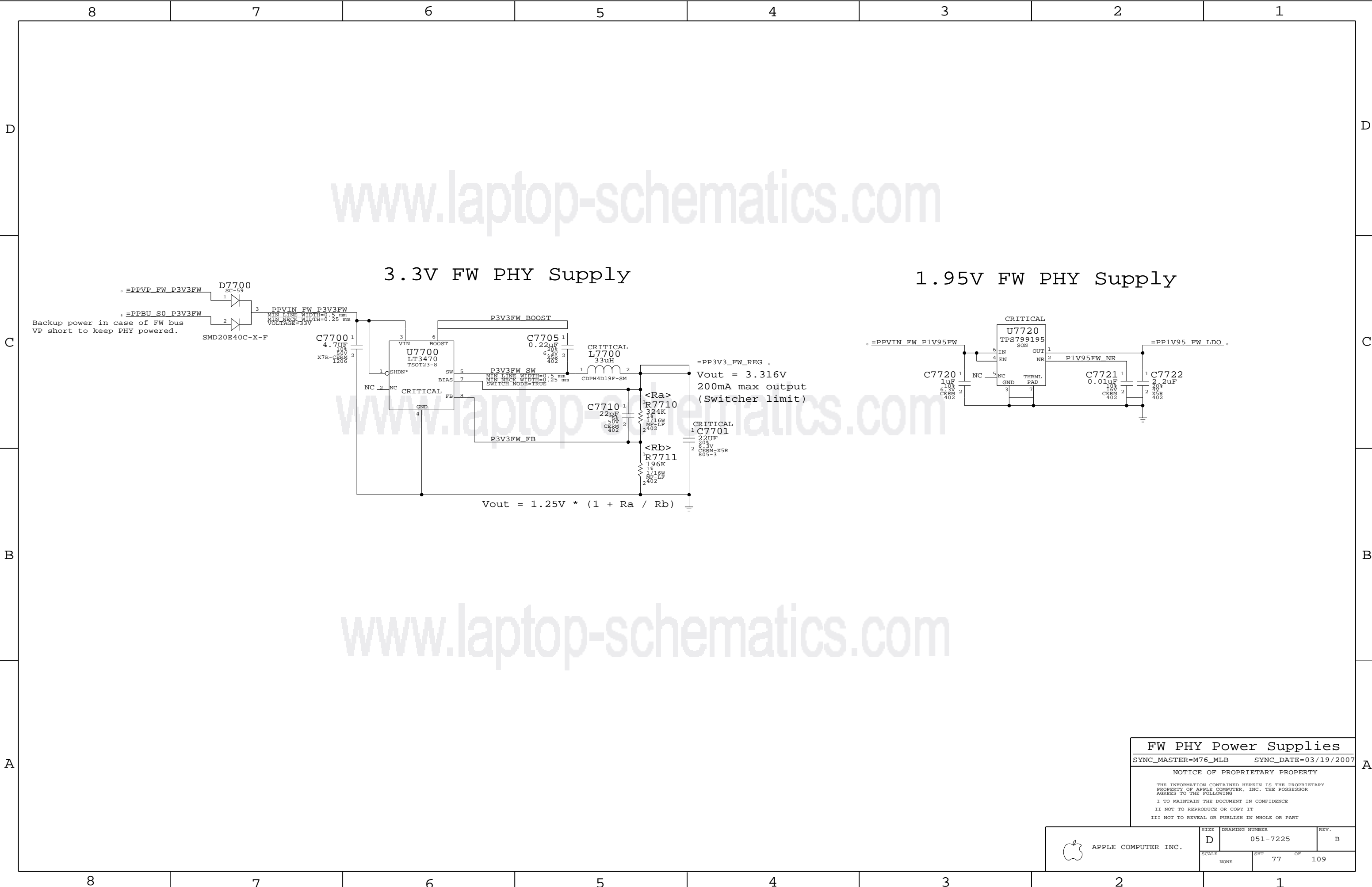
SIZE D      DRAWING NUMBER 051-7225      REV. B

SCALE NONE      SHT 75 OF 109



1.5V Power Supply  
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007  
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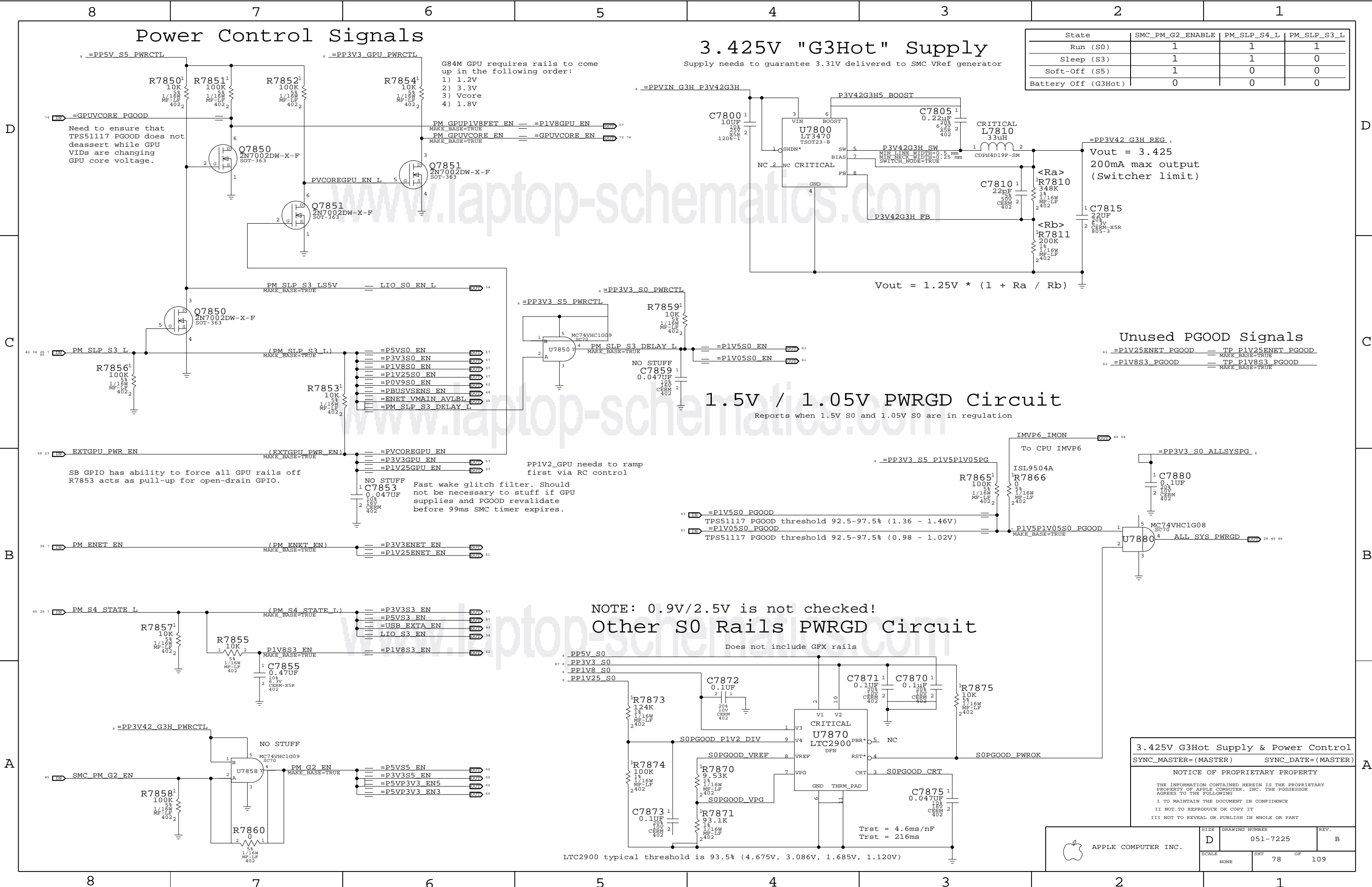
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FW PHY Power Supplies		
SYNC_MASTER=M76_MLB		SYNC_DATE=03/19/2007
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NONE		77	109



Power Control Signals

3.425V "G3Hot" Supply

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Vout = 3.425  
200mA max output  
(Switcher limit)

Unused PGOOD Signals

=P1V25ENET PGOOD	= TP P1V25ENET PGOOD
=P1V8S3 PGOOD	= TP P1V8S3 PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

NOTE: 0.9V/2.5V is not checked!  
Other S0 Rails PWRGD Circuit

Does not include GFX rails

3.425V G3Hot Supply & Power Control

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	B
SCALE	NONE	SHT	78 OF 109

## Page Notes

Power aliases required by this page:

- =PPIV2\_GPU\_PEX\_PLLXVDD
- =PPIV2\_GPU\_PEX\_IOVDDQ
- =PPIV2\_GPU\_PEX\_IOVDD

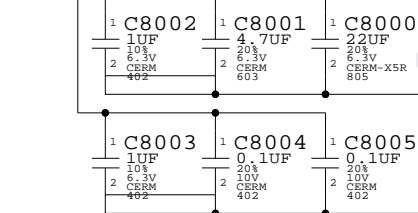
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BOM options provided by this page:  
(NONE)

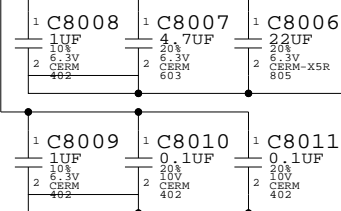
=PPIV2\_GPU\_PEX\_PLLXVDD  
=PPIV2\_GPU\_PEX\_IOVDDQ  
=PPIV2\_GPU\_PEX\_IOVDD

PEX 1.2V Current = 2A

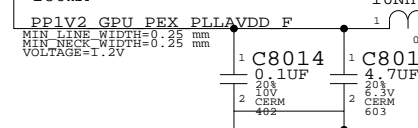
250mA



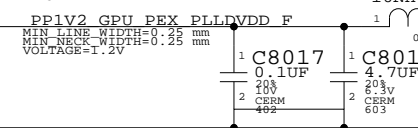
1500mA



180mA



20mA



OMIT  
U8000  
NB8P-GS-W-A2  
BGA  
(1 OF 8)

PCI-EXPRESS BUS INTERFACE



NV G84M PCI-E

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SCALE NONE SHT 80 OF 109

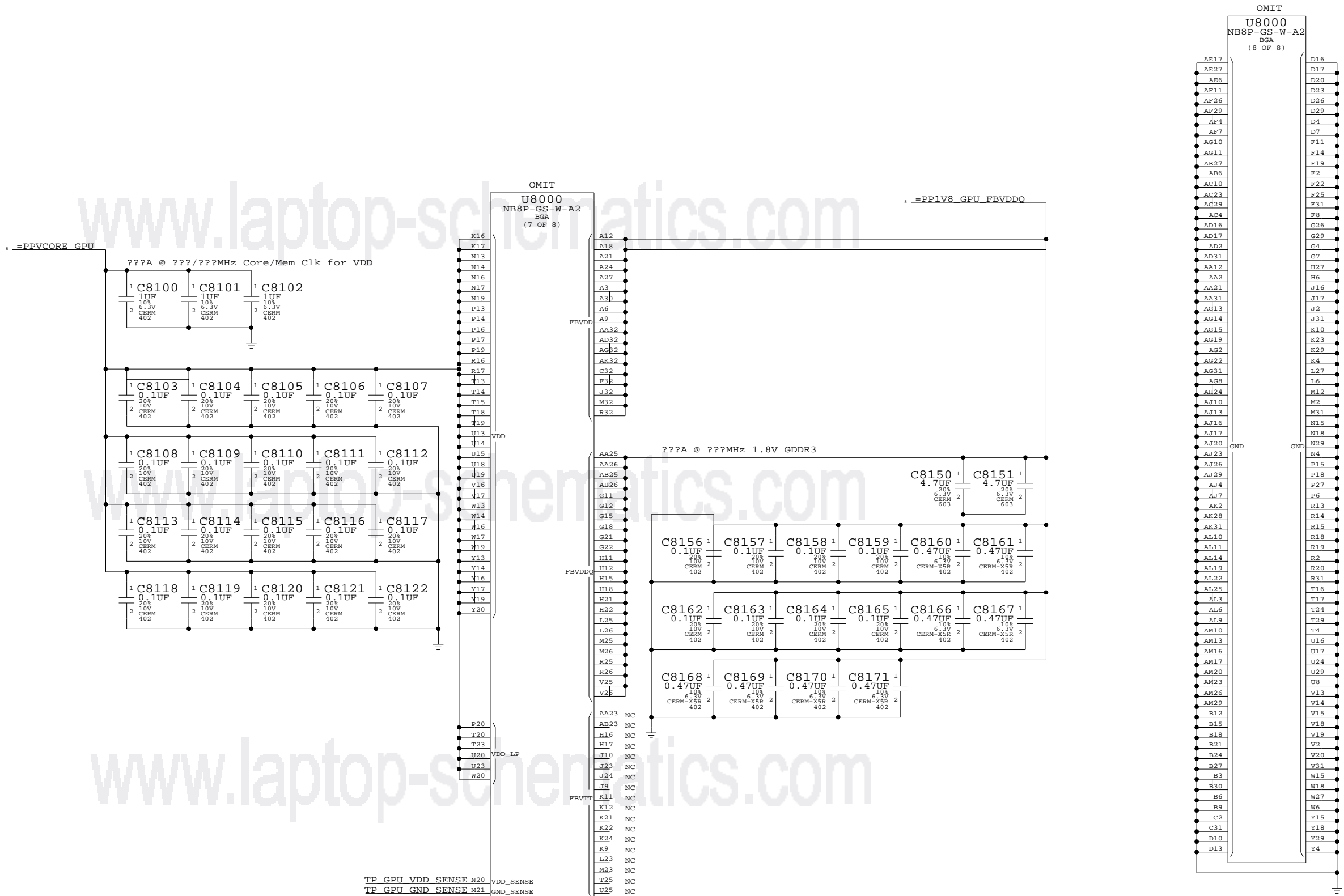


Page Notes

Power aliases required by this page:  
- =PPVCORE\_GPU  
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



NV G84M Core/FB Power

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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NONE	81	109



Power aliases required by this page:  
- =PP1V8\_S0\_FB\_VDD  
- =PP1V8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

GDDR3 Frame Buffer A

SYNC\_MASTER= (MASTER) SYNC\_DATE= (MASTER)

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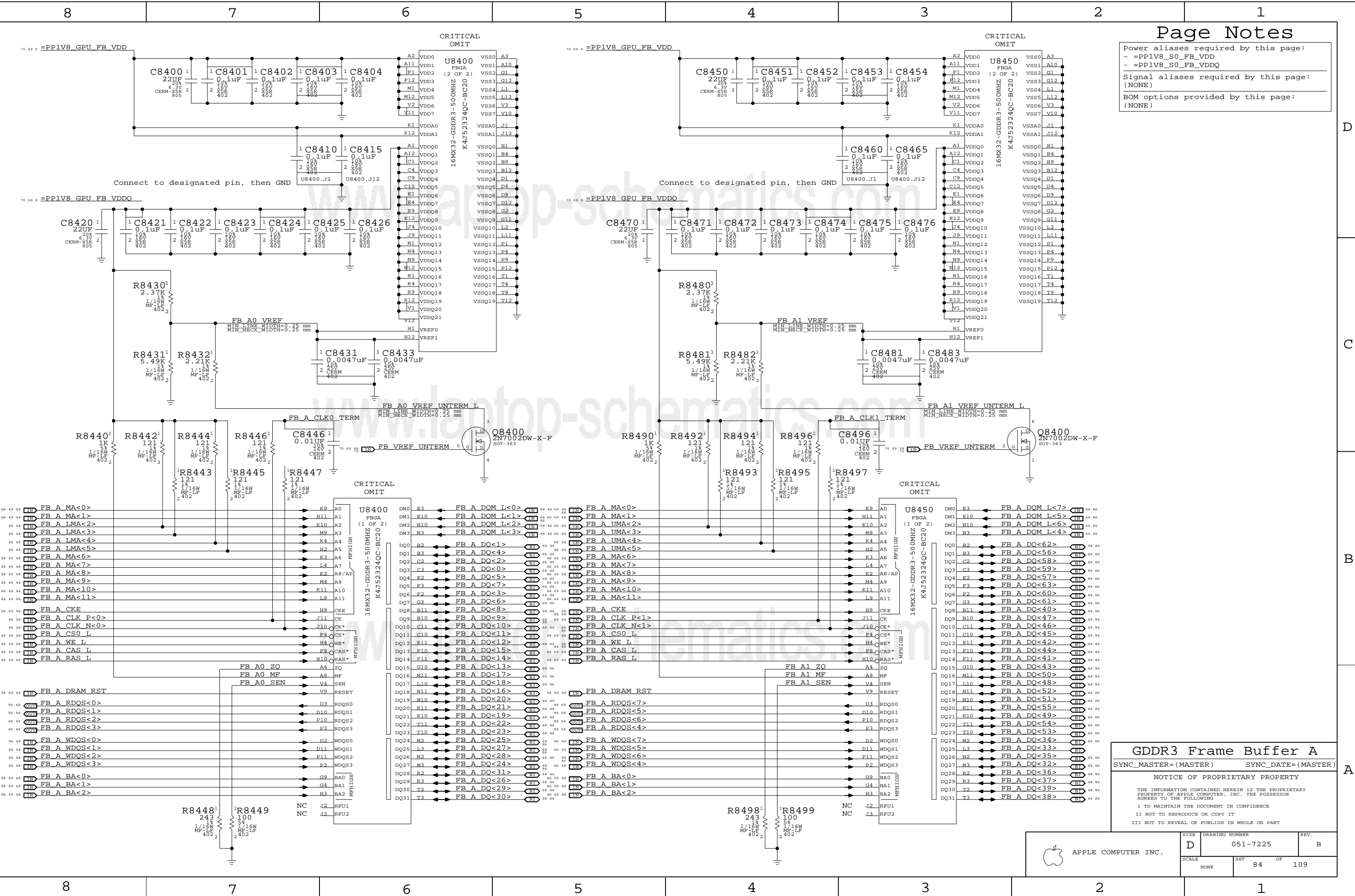
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	B
SCALE	SHT	OF
NONE	84	109





Power aliases required by this page:  
- =PP1V8\_S0\_FB\_VDD  
- =PP1V8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
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BOM options provided by this page:  
(NONE)

GDDR3 Frame Buffer B

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

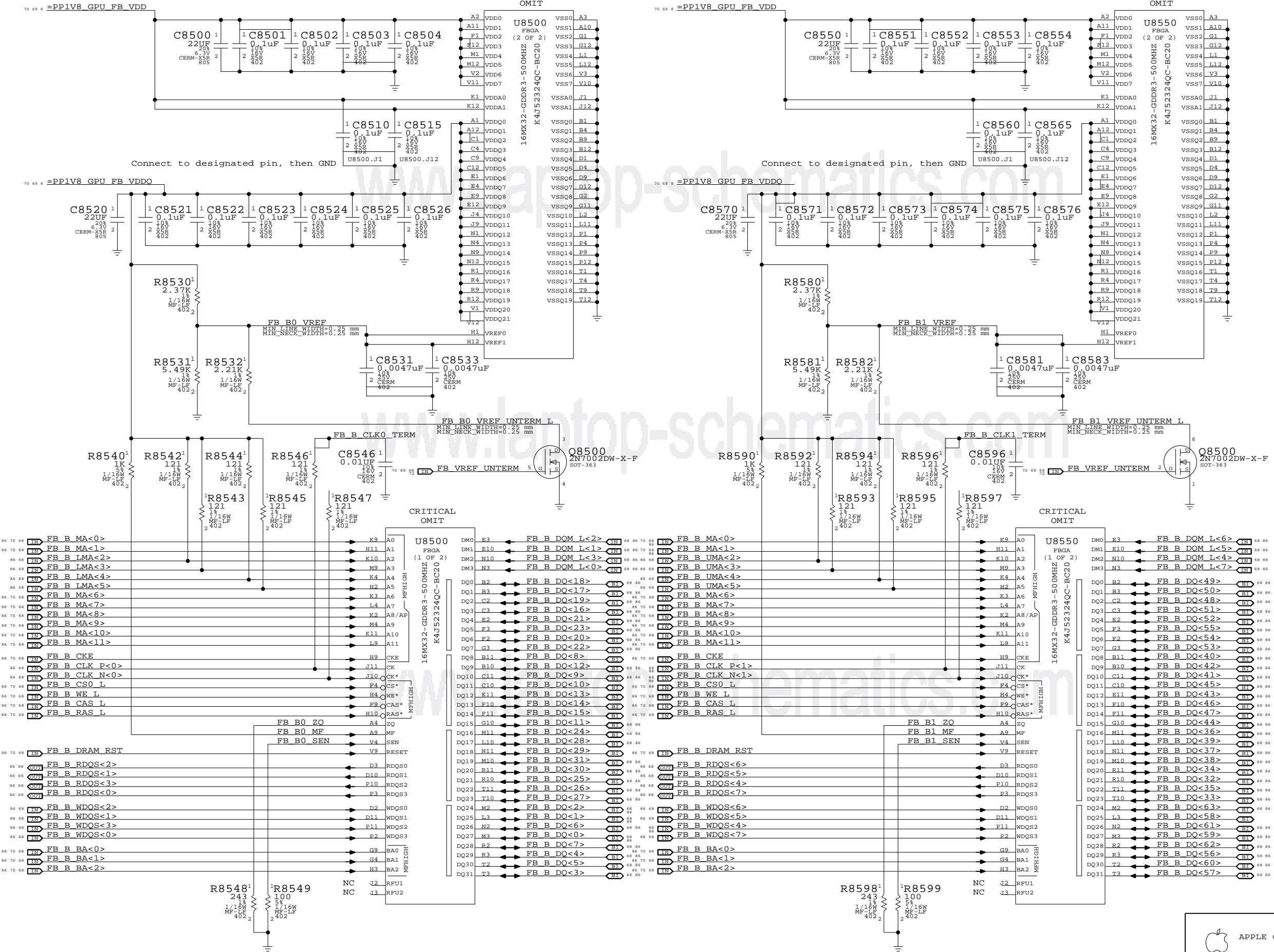
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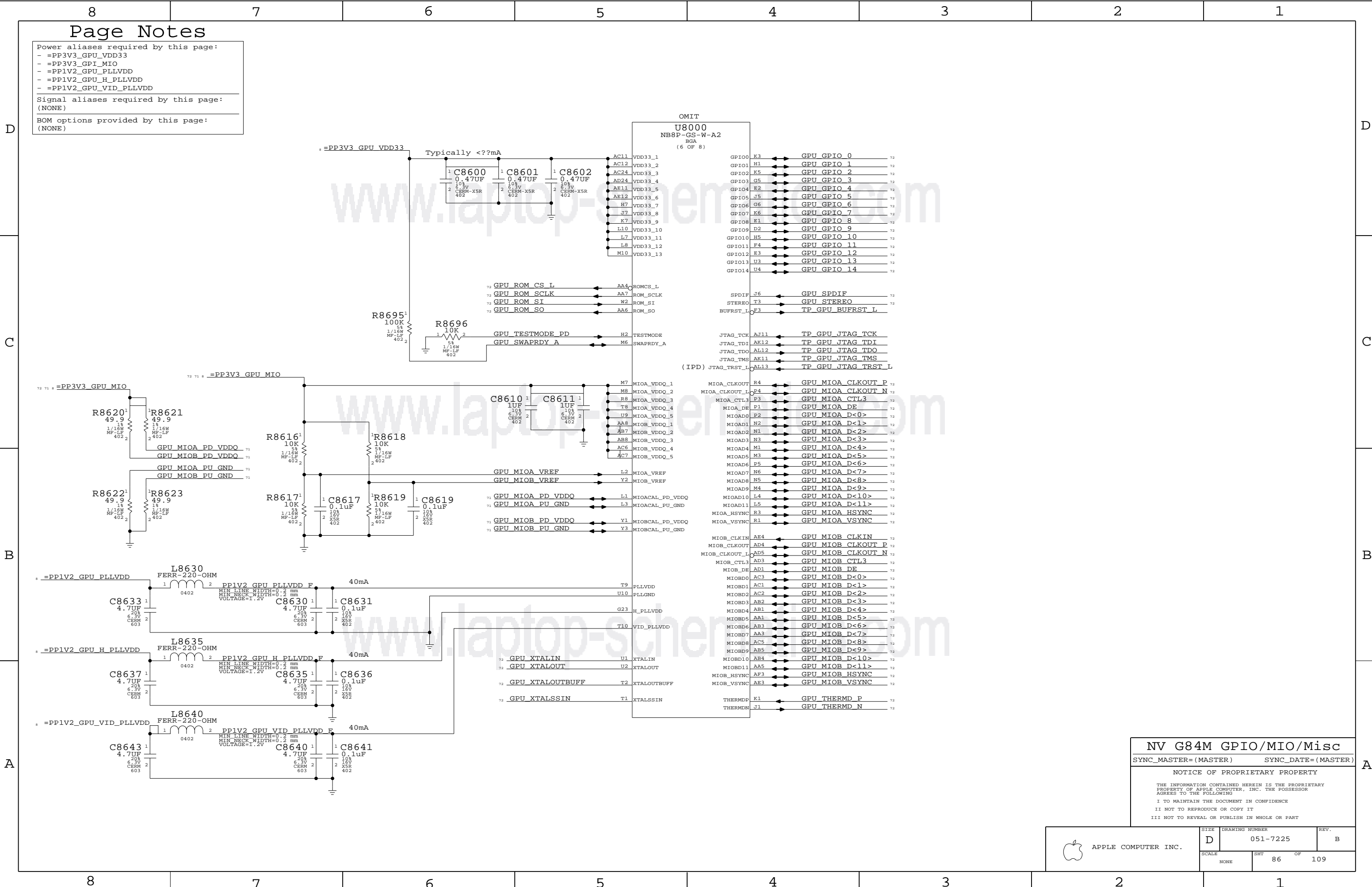
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D	051-7225	B
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NONE	85	109





# Page Notes

Power aliases required by this page:

- =PP3V3\_GPU\_VDD33
- =PP3V3\_GPU\_MIO
- =PP1V2\_GPU\_PLLVDD
- =PP1V2\_GPU\_H\_PLLVDD
- =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

## NV G84M GPIO/MIO/Misc

SYNC\_MASTER= (MASTER) SYNC\_DATE= (MASTER)

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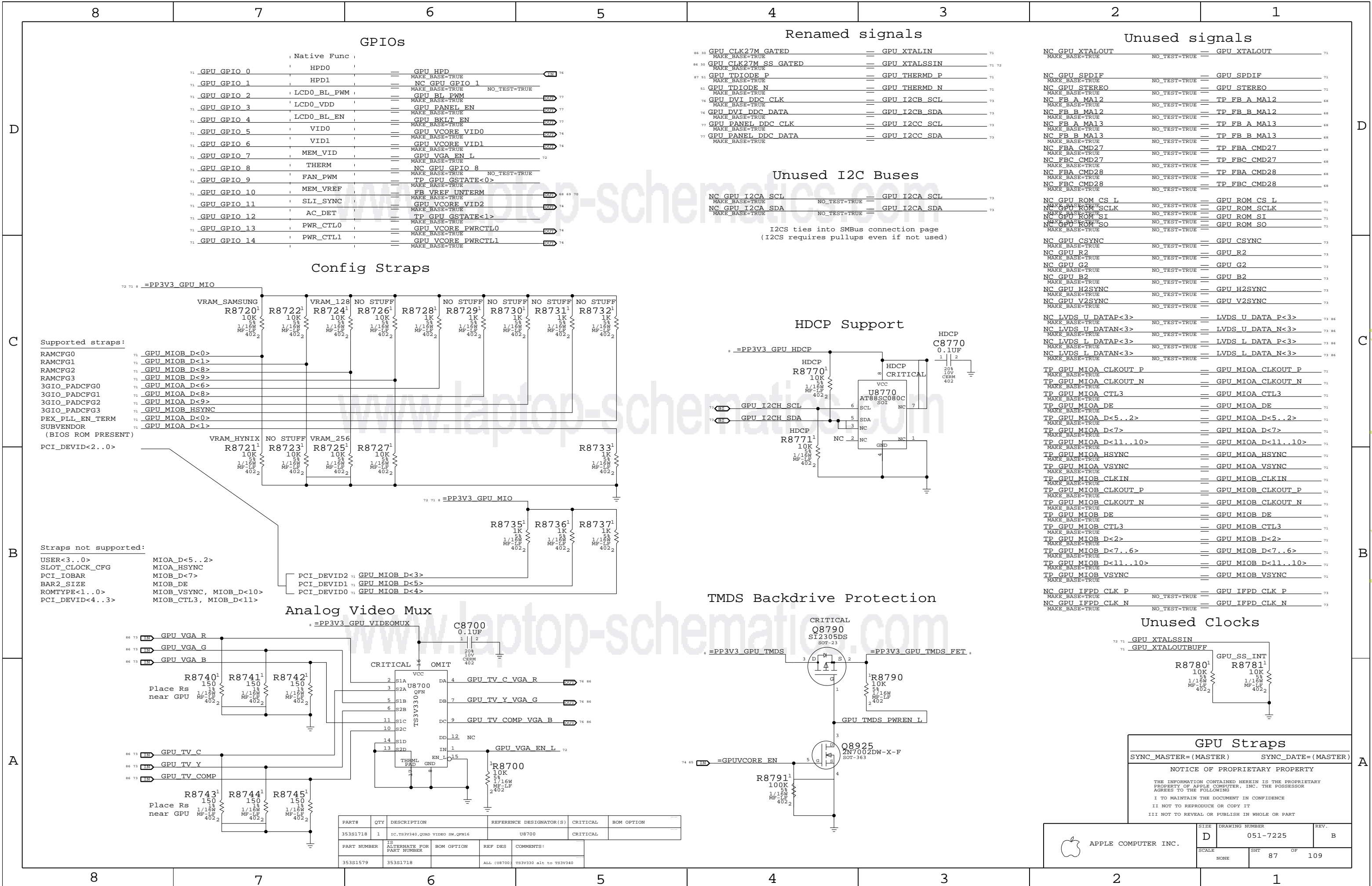
109

NONE

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109





Page Notes

Power aliases required by this page:

- =PP1V8\_GPU\_IFPX  
- =PP3V3\_GPU\_IFPCD\_IOVDD  
- =PP3V3\_GPU\_DAC

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

Sum of peak currents: 240mA

=PP1V8\_GPU\_IFPX

=PP3V3\_GPU\_IFPCD\_IOVDD

Sum of peak currents: 390mA

=PP3V3\_GPU\_DAC

I2CS must be pulled up if not used  
I2CS addr fixed at 0x9E,0x9F

NV G84M Video Interfaces

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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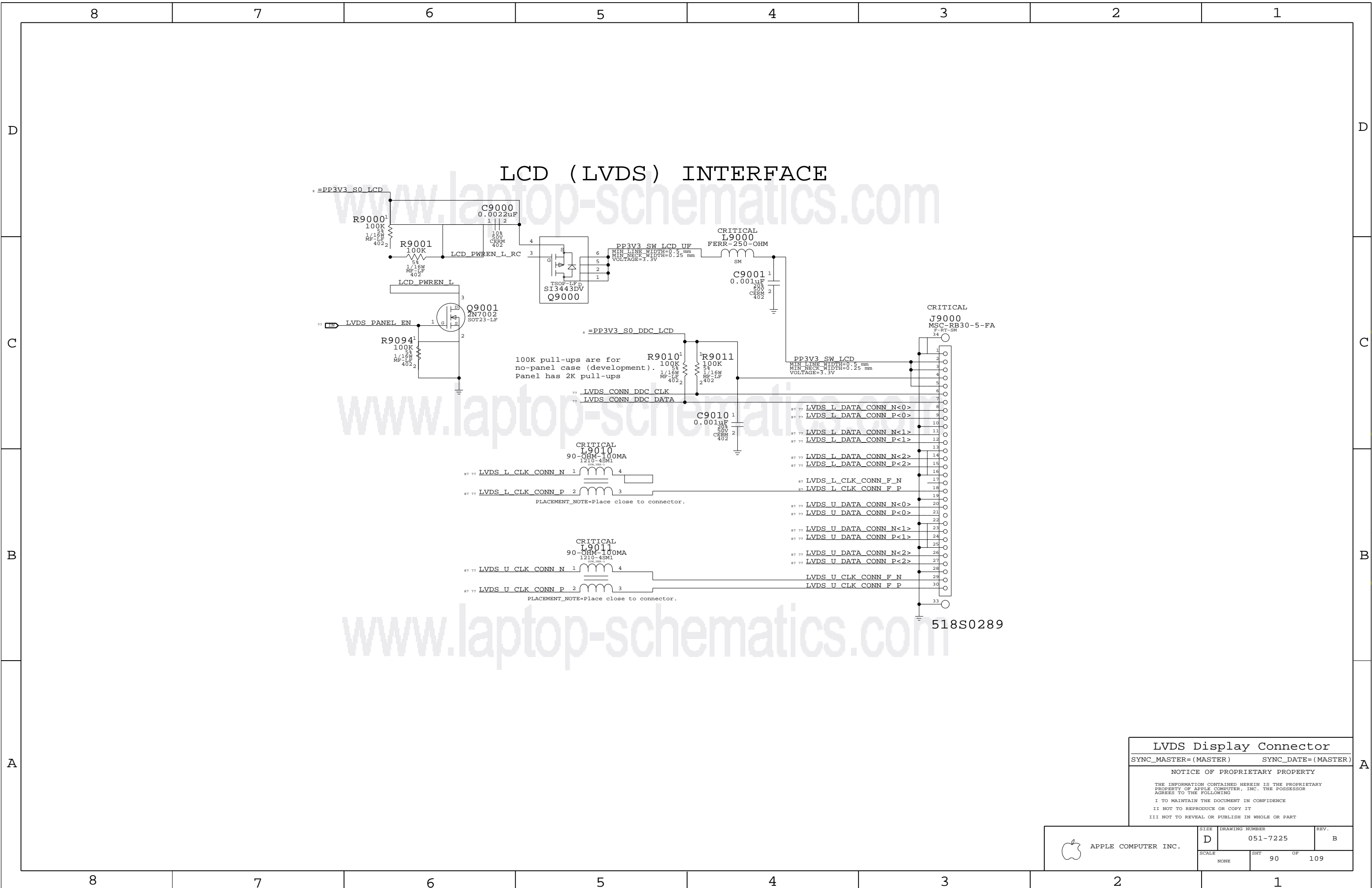
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LVD5 Display Connector

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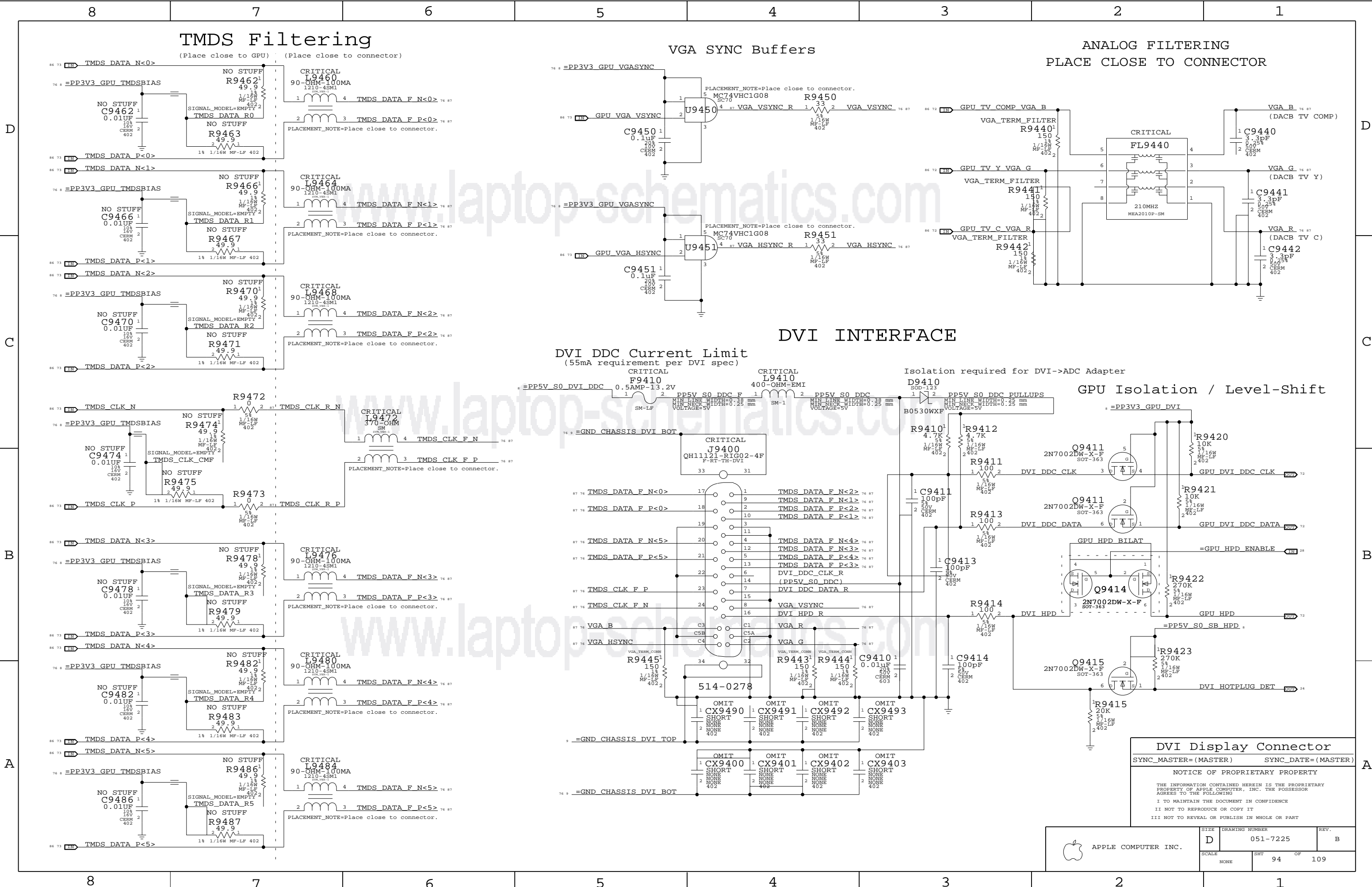
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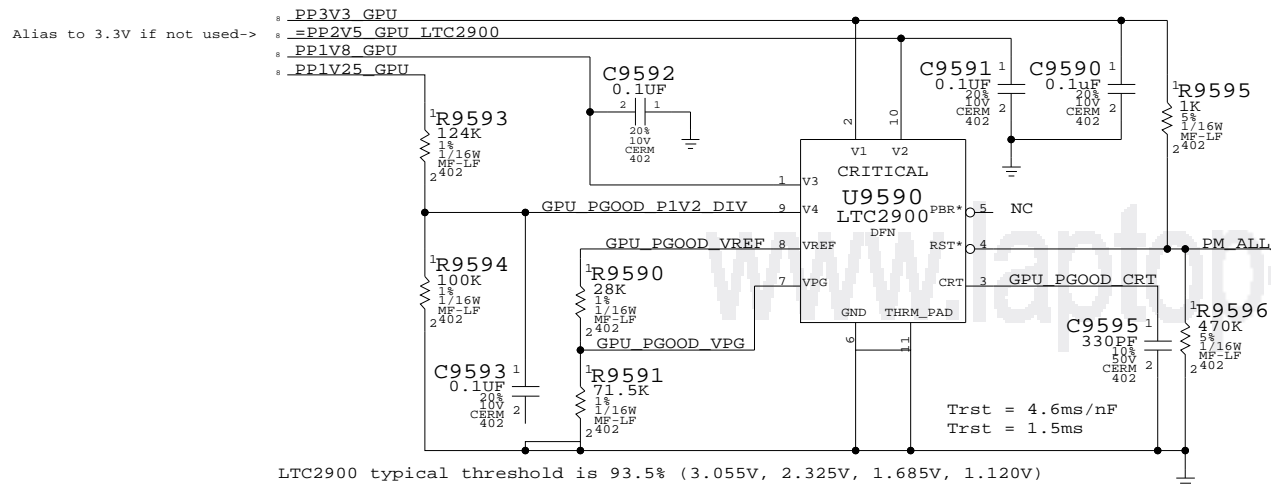






## PGOOD Monitor for GPU Rails

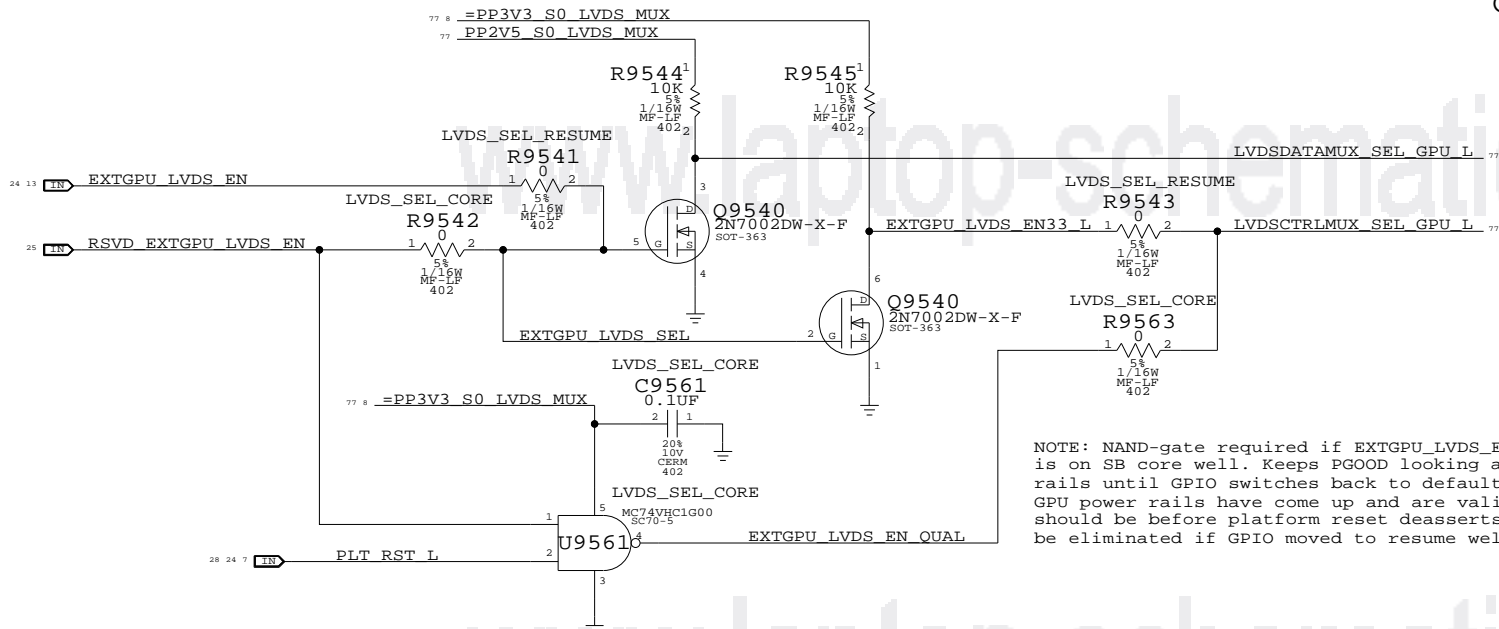
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

NB LVDS I/F

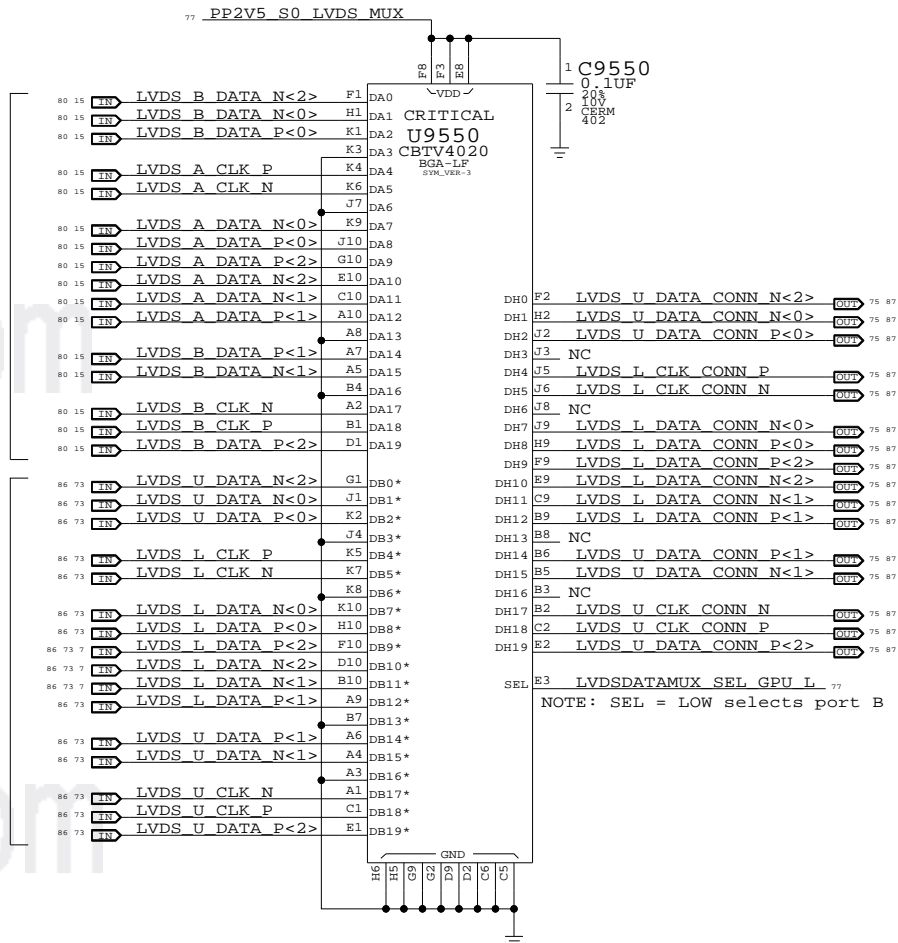
## Mux Select Conditioning



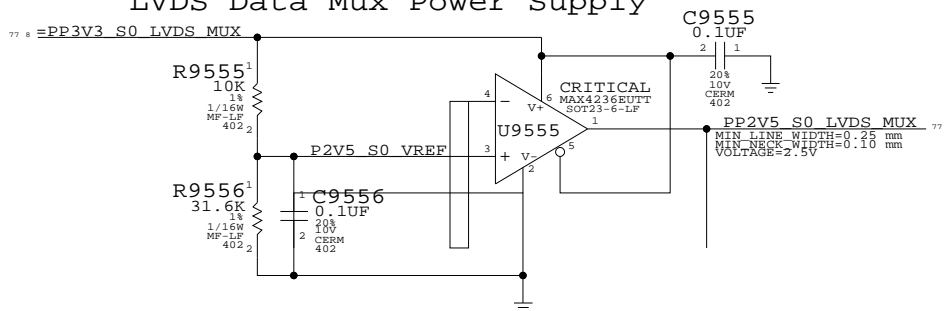
NOTE: NAND-gate required if EXTGPU LVDS\_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

GPU LVDS I/F

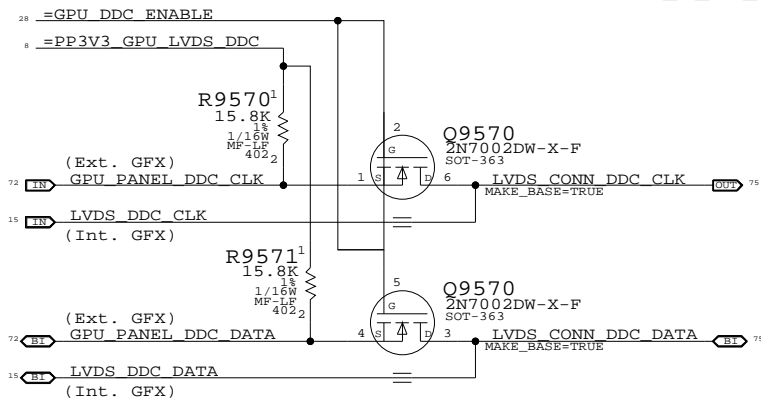
## LVDS I/F Mux



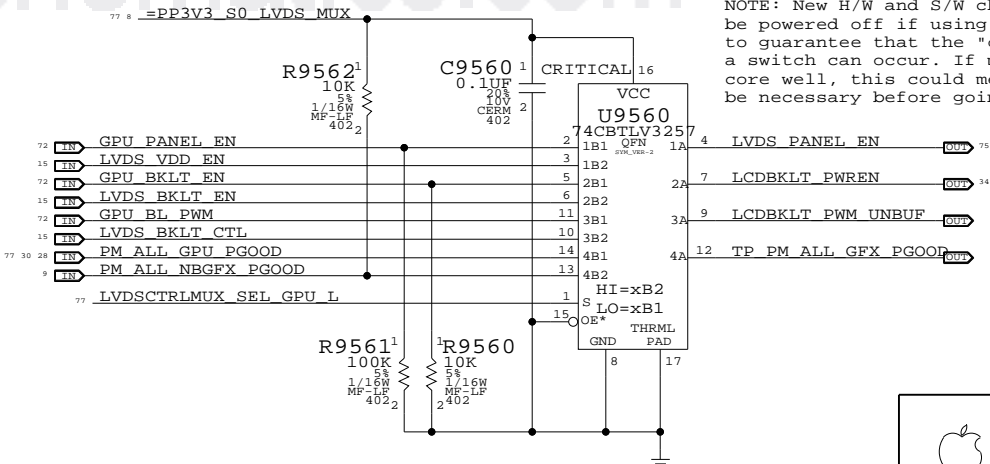
## LVDS Data Mux Power Supply



## GPU DDC Pass FETs



## Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

## LVDS Interface Mux

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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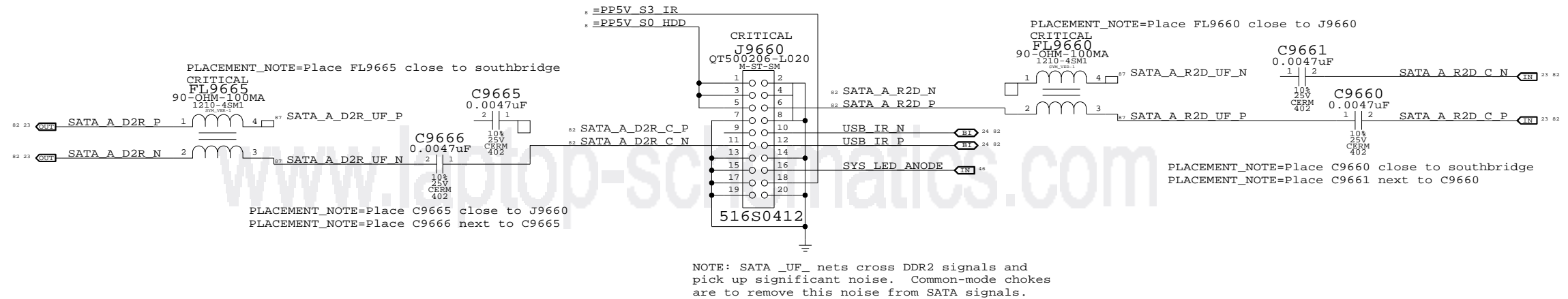
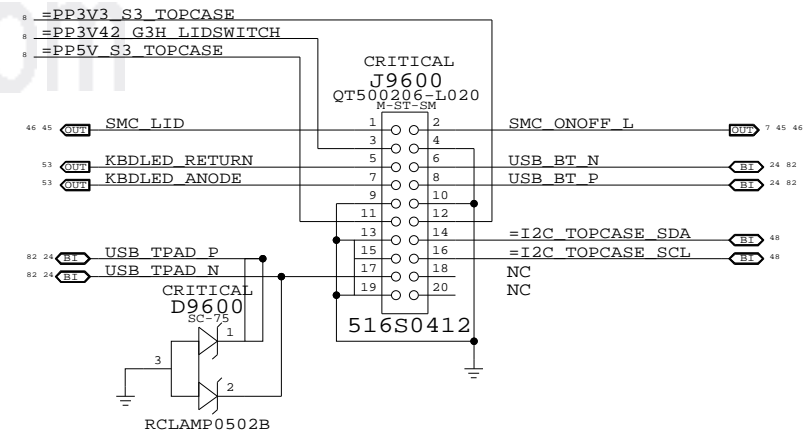
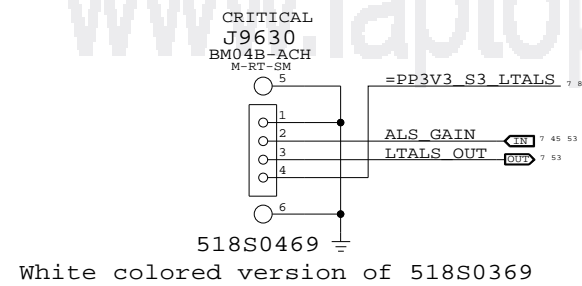
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Project Specific Connectors	
SYNC_MASTER=(M59_SYNC)	SYNC_DATE=08/24/2006

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	NONE	96	109

8		7		6		5		4		3		2		1	
FSB (Front-Side Bus) Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
FSB_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
FSB_DSTB_55S		*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
FSB_ADDR		*	=3:1_SPACING	?											
FSB_ADDR2ADDR		*	=2:1_SPACING	?											
FSB_ADSTB		*	=3:1_SPACING	?											
FSB_ADDR2ADSTB		*	=3:1_SPACING	?											
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
FSB_COMMON		*	=2:1_SPACING	?											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
FSB_ADDR		FSB_ADDR	*	FSB_ADDR2ADDR											
FSB_ADDR		FSB_ADSTB	*	FSB_ADDR2ADSTB											
FSB_DATA		FSB_DATA	*	FSB_DATA2DATA											
FSB_DATA		FSB_DSTB	*	FSB_DATA2DSTB											
All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs. Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers. NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened. SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3															
CPU Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
CPU_27P4S		*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL							
CPU_55S		*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
CPU_2TO1		*	=2:1_SPACING	?											
CPU_COMP		*	25 MIL	?											
CPU_GTLREF		*	25 MIL	?											
CPU_ITP		*	=2:1_SPACING	?											
CPU_VCCSENSE		*	25 MIL	?											
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance. DG recommends at least 25 mils, >50 mils preferred															
Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance. SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4															
CPU / FSB Net Properties															
ELECTRICAL_CONSTRAINT_SET		PHYSICAL		SPACING											
FSB_COMMON		FSB_55S	FSB_COMMON	FSB ADS L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB BNR L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB BPRI L		10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB BREQ0 L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB DBSY L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB DEFER L		10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB DPWR L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB DRDY L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB HIT L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB HITM L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB LOCK L		7 10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB RS L<2..0>		10 14									
FSB_COMMON		FSB_55S	FSB_COMMON	FSB TRDY L		10 14									
FSB_CPURST_L		FSB_55S	FSB_COMMON	FSB CPURST L		7 10 13 14									
FSB_DATA_GROUP0		FSB_55S	FSB_DATA	FSB D L<15..0>		7 10 14									
FSB_DATA_GROUP0		FSB_55S	FSB_DATA	FSB DINV L<0>		7 10 14									
FSB_DSTB0		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>		7 10 14									
FSB_DSTB0		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>		7 10 14									
FSB_DATA_GROUP1		FSB_55S	FSB_DATA	FSB D L<31..16>		7 10 14									
FSB_DATA_GROUP1		FSB_55S	FSB_DATA	FSB DINV L<1>		7 10 14									
FSB_DSTB1		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>		7 10 14									
FSB_DSTB1		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>		7 10 14									
FSB_DATA_GROUP2		FSB_55S	FSB_DATA	FSB D L<47..32>		7 10 14									
FSB_DATA_GROUP2		FSB_55S	FSB_DATA	FSB DINV L<2>		7 10 14									
FSB_DSTB2		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>		7 10 14									
FSB_DSTB2		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>		7 10 14									
FSB_DATA_GROUP3		FSB_55S	FSB_DATA	FSB D L<63..48>		7 10 14									
FSB_DATA_GROUP3		FSB_55S	FSB_DATA	FSB DINV L<3>		7 10 14									
FSB_DSTB3		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>		7 10 14									
FSB_DSTB3		FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>		7 10 14									
FSB_ADDR_GROUP0		FSB_55S	FSB_ADDR	FSB A L<16..3>		7 10 14									
FSB_ADDR_GROUP0		FSB_55S	FSB_ADDR	FSB REQ L<4..0>		7 10 14									
FSB_ADSTB0		FSB_55S	FSB_ADSTB	FSB ADSTB L<0>		7 10 14									
FSB_ADDR_GROUP1		FSB_55S	FSB_ADDR	FSB A L<35..17>		7 10 14									
FSB_ADSTB1		FSB_55S	FSB_ADSTB	FSB ADSTB L<1>		7 10 14									
CPU_IERR_L		CPU_55S		CPU IERR L		10									
CPU_FERR_L		CPU_55S		CPU FERR L		10 23									
CPU_PROCHOT_L		CPU_55S	CPU_2TO1	CPU PROCHOT L		10 46 58									
CPU_PWRGD		CPU_55S		CPU PWRGD		7 10 13 23									
CPU_FROM_SB		CPU_55S		CPU INTR		10 23									
CPU_FROM_SB		CPU_55S		CPU NMI		10 23									
CPU_FROM_SB		CPU_55S		CPU A20M L		10 23									
CPU_FROM_SB		CPU_55S		CPU DPSLP L		7 10 23									
CPU_FROM_SB		CPU_55S		CPU IGNNE L		10 23									
CPU_INIT_L		CPU_55S		CPU INIT L		10 23 47									
CPU_FROM_SB		CPU_55S		CPU SMI L		10 23									
CPU_FROM_SB		CPU_55S		CPU STPCLK L		7 10 23									
PM_THRMTRIP_L		CPU_55S	CPU_2TO1	PM THRMTRIP L		10 16 23 46									
FSB_CPUSLP_L		CPU_55S		FSB CPUSLP L		7 10 14									
PM DPRSLPVR		CPU_55S	CPU_2TO1	PM DPRSLPVR		7 16 25 58									
(See above)		CPU_55S	CPU_2TO1	IMVP DPRSLPVR		7 58									
CPU_BSEL0		CPU_55S	CPU_2TO1	CPU BSEL<0>		10 30									
(See above)		CPU_55S	CPU_2TO1	NB BSEL<0>		13 16 30									
CPU_BSEL1		CPU_55S	CPU_2TO1	CPU BSEL<1>		10 30									
(See above)		CPU_55S	CPU_2TO1	NB BSEL<1>		13 16 30									
CPU_BSEL2		CPU_55S	CPU_2TO1	CPU BSEL<2>		10 30									
(See above)		CPU_55S	CPU_2TO1	NB BSEL<2>		13 16 30									
CPU DPRSTP_L		CPU_55S	CPU_2TO1	CPU DPRSTP L		7 10 16 23 58									
CPU_GTLREF		CPU_55S	CPU_GTLREF	CPU GTLREF		10									
CPU_COMP		CPU_55S	CPU_COMP	CPU COMP<3>		10									
CPU_COMP		CPU_27P4S	CPU_COMP	CPU COMP<2>		10									
CPU_COMP		CPU_55S	CPU_COMP	CPU COMP<1>		10									
CPU_COMP		CPU_27P4S	CPU_COMP	CPU COMP<0>		10									
XDP_TDI		CPU_55S	CPU_ITP	XDP TDI		10 13									
XDP_TDO		CPU_55S	CPU_ITP	XDP TDO		10 13									
XDP_TMS		CPU_55S	CPU_ITP	XDP TMS		10 13									
XDP_TCK		CPU_55S	CPU_ITP	XDP TCK		10 13									
XDP_TRST_L		CPU_55S	CPU_ITP	XDP TRST L		10 13									
XDP_BEN_L		CPU_55S	CPU_ITP	XDP BPM L<4..0>		10 13									
XDP_BEN_L5		CPU_55S	CPU_ITP	XDP BPM L<5>		10 13									
		CLK_FSB_100D	CLK_FSB	XDP CLK_P		13 30 84									
		CLK_FSB_100D	CLK_FSB	XDP CLK_N		13 30 84									
(FSB_CPURST_L)		CPU_55S	CPU_ITP	XDP CPURST L		13									
		CPU_55S	CPU_2TO1	CPU VID<6..0>		11 12									
		CPU_55S	CPU_2TO1	IMVP6_VID<6..0>		7 12 48									
CPU_VCCSENSE		CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P		11 58									
CPU_VCCSENSE		CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N		11 58									
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P		58									
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N		58									
CPU/FSB Constraints															
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## DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM\_\*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK	MEM_CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK	MEM_CLK N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CS L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_DATA	MEM_A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<0>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<1>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<2>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<3>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<4>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<5>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<6>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS P<7>	17 31
	MEM_85D	MEM_DQS	MEM_DQS	MEM_A DQS N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK	MEM_CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK	MEM_CLK N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CS L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_DATA	MEM_B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<0>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<1>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<2>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<3>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<4>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<5>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<6>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS P<7>	17 32
	MEM_85D	MEM_DQS	MEM_DQS	MEM_B DQS N<7>	17 32

## Memory Constraints

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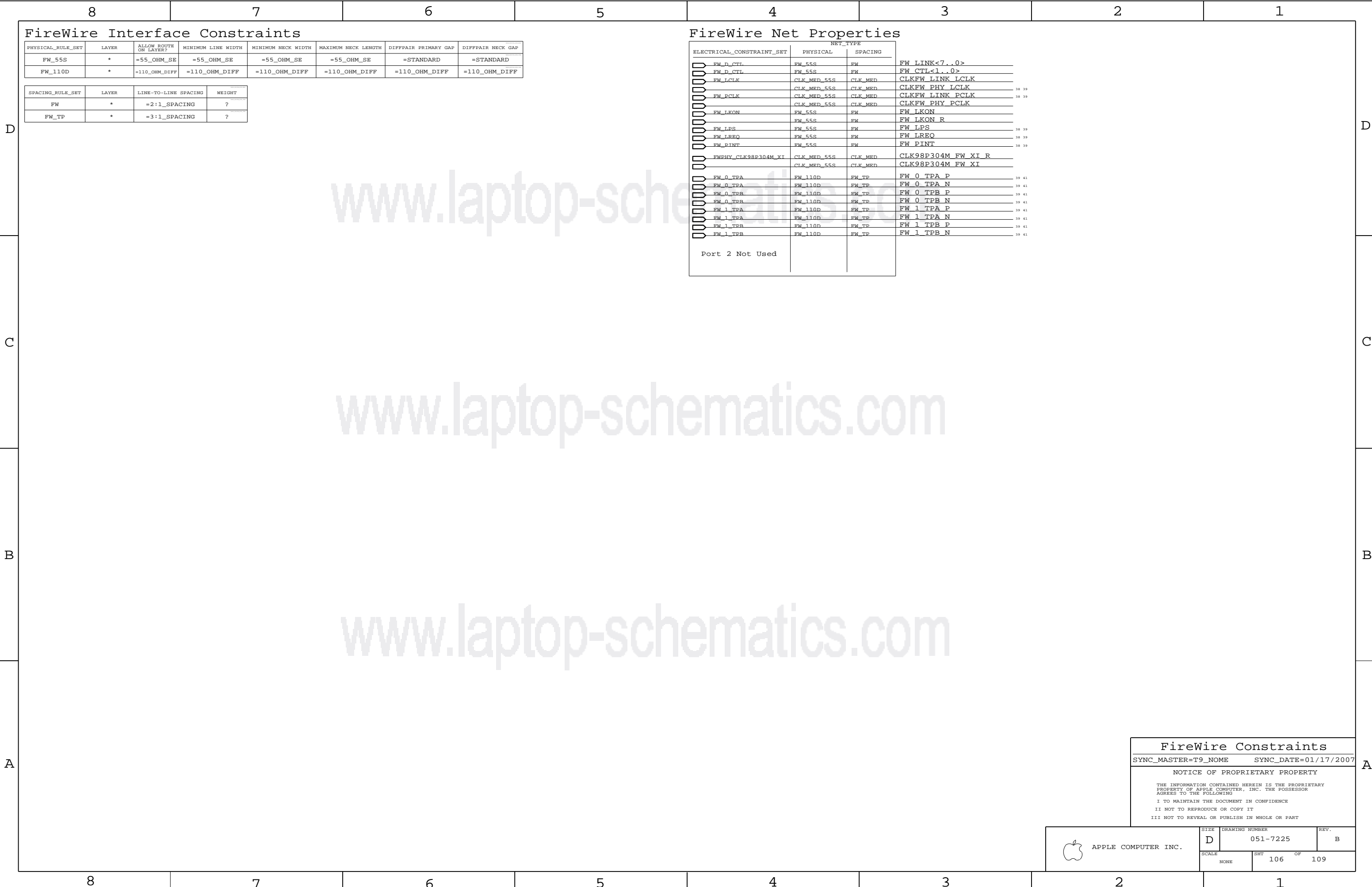
NONE	102	109
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ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L	23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDIOW L	23 42
IDE_PDIOI_L	IDE_55S	IDE	IDE_PDIOI R	23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDACK L	23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDREO	23 42
IDE_PDIOIRDY	IDE_55S	IDE	IDE_PDIOIRDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L	24 42
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